UNIVERSITI PUTRA MALAYSIA

SELF-BIASING MULTIPLE-GATED-TRANSISTORS METHOD IN DESIGNING LOW-NOISE AMPLIFIER AND THIRD-ORDER CHEBYSHEV FILTER

ARASH ABBASI

FK 2015 8

SELF-BIASING MULTIPLE-GATED-TRANSISTORS METHOD IN DESIGNING LOW-NOISE AMPLIFIER AND THIRD-ORDER CHEBYSHEV FILTER

By

ARASH ABBASI

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Master of Science

June 2015

DEDICATION

I dedicate this thesis first and foremost to mom, dad for their financial support and love throughout those two years spent in Malaysia. I also dedicate this thesis to my sister and brother for the laughs, encouragement, admiration, and all the love and strength you always give me.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

SELF-BIASING MULTIPLE-GATED-TRANSISTORS METHOD IN DESIGNING LOW-NOISE AMPLIFIER AND THIRD-ORDER CHEBYSHEV FILTER

By

ARASH ABBASI

June 2015

Chairman : Nasri b. Sulaiman. PhD
Faculty : Engineering

Analog filters and low noise amplifiers (LNAs) are extensively employed in the receiver front-end structure of the CMOS radio frequency (RF) applications. One of the analog filters usually employed in CMOS RF is Gm-C filter which consists of transconductor (Gm or OTA) block and capacitor (C). The OTA is the main building block of the Gm-C filter that the characteristics of the Gm-C filter is related to its performance. While several techniques are reported to design OTA, its major limitation is its poor linearity and complexity of the design. In addition, the LNA is modified to achieve sufficient linearity, reduce complexity of the design and lower noise figure (NF) to suppress the noise from the first stage of the receiver.

In this dissertation, a self-biasing multiple-gated-transistors (MGTR) method is modified to improve the linearity of the OTA and LNA. Self-biasing reduce the complexity of the design and number of components. The basic concept of the MGTR method is utilizing two transistors in order to remove the third-order harmonics of each other. Each of these transistors must be biased in different region. Thus, two external biasing is needed. However, the number of external biasing is reduced by self-biasing modification.

The modified method is used to modify an OTA for the Gm-C filter. Then, the Gm-C filter is used by third-order Chebyshev filter to prepare the requirements of direct-conversion receiver for digital television (DTV). The modified OTA is designed in 90 nm CMOS technology. The simulation result with two-tone test at 100 MHz center frequency shows that the third-order Chebyshev filter with modified OTA has 8 dBm Input-referred Third-Order Intercept Point (IIP3) improvement compared with the third-order Chebyshev filter with single-gate OTA. The third-order Chebyshev filter with modified OTA is operating between 50-200 MHz cutoff frequencies. Moreover, it achieves maximum NF of 13.5 dB and maximum IIP3 of approximately 17.3 dBm at 100 MHz, whereas consuming 18 mA with 1.2 V supply voltage.

Furthermore, the modified LNA is operating between 900-2400 MHz cutoff frequencies. The simulation result with two-tone test at 2.1 GHz sample center frequency shows that the modified LNA has 10 IIP3 improvement compared with a single-gate LNA. The modified LNA achieves maximum NF of 1.9 dB, 9 dB Gain and maximum IIP3 of approximately 13.5 dBm, whereas consuming 3.9 mA with 2 V supply voltage.

Abstrak bagi tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan pengijazahan Ijazah Master Sains

KAEDAH TRANSISTOR GET BERGANDA PINCANGAN-KENDIRI DALAM MEREKA-BENTUK PENGUAT HINGAR RENDAH DAN PENAPIS CHEBYSHEV ATURAN KETIGA

Oleh

ARASH ABBASI

Jun 2015

Pengerusi : Nasri b. Sulaiman. PhD
Fakulti : Kejuruteraan

Penapis analog dan amplifier hingar rendah (LNAs) telah digunakan secara meluas dalam struktur bahagian hadapan penerima bagi aplikasi frekuensi radio (RF) CMOS. Salah satu penapis analog yang lazimnya digunakan dalam CMOS RF adalah penapis Gm-C yang terdiri daripada blok transkonduktor (Gm atau OTA) dan kapasitor (C). OTA adalah blok binaan utama bagi penapis Gm-C yang mana ciri-ciri penapis Gm-C itu berhubung kait dengan prestasinya. Sungguhpun terdapat beberapa teknik yang digunakan untuk mereka bentuk OTA, batasan utamanya adalah kelinearannya yang teruk dan kerumitan dalam mereka bentuk. Tambahan pula, LNA diubah suai untuk mendapatkan kelinearan yang dikehendaki, mengurangkan kerumitan reka bentuk dan mengurangi nilai hingar (NF) untuk menyekat bunyi dari peringkat pertama penerima.

Dalam disertasi ini, satu kaedah transistor get berganda pincang sendiri (MGTR) telah diubah suai untuk meningkatkan kelinearan OTA dan LNA. Pincang sendiri mampu mengurangkan kerumitan reka bentuk dan bilangan komponen yang terlibat. Konsep asas bagi kaedah MGTR adalah penggunaan dua transistor untuk membuang harmonik tertib ketiga antara satu sama lain. Setiap satu transistor ini mesti dipincangkan dalam kawasan yang berbeza. Dengan yang demikian, dua pincangan luaran diperlukan. Walau bagaimanapun, bilangan pincangan luaran dapat dikurangkan melalui pengubahsuaian pincang sendiri.

Kaedah yang diubah suai ini digunakan untuk mengubah satu OTA bagi penapis Gm-C. Kemudiannya, penapis Gm-C tersebut digunakan oleh penapis Chebyshev tertib ketiga untuk menyediakan keperluan kepada penerima pertukaran bagi televisyen digital (DTV). OTA yang terubah suai direka bentuk dalam teknologi CMOS 90 nm. Keputusan simulasi dengan ujian dua-nada pada frekuensi pusat 100 MHz menunjukan bahawa penapis Chebyshev tertib ketiga dengan OTA terubah suai mempunyai peningkatan input-dirujuk Titik Pintasan Tertib Ketiga (IIP3) 8 dBm berbanding penapis Chebyshev tertib ketiga bagi OTA get-tunggal. Penapis Chebyshev tertib ketiga dengan OTA terubah suai beroperasi di antara frekuensi potong 50-200 MHz. Selain itu, ia mencapai NF maksimum 13.5 dB dan IIP3 maksimum lebih kurang 17.3 dBm pada 100 MHz, dengan menggunakan 18 mA dengan voltan bekalan 1.2 V.

Tambahan lagi, LNA terubah suai beroperasi di antara frekuensi potong 900-2400 MHz. Keputusan simulasi dengan ujian dua-nada pada sampel frekuensi pusat 2.1 GHz menunjukkan bahawa LNA terubah suai mempunyai peningkatan 10 IIP3 berbanding LNA get-tunggal. LNA terubah suai mencapai NF maksimum 1.9 dB, Tambahan 9 dB dan IIP3 maksimum lebih kurang 13.5 dBm, menggunakan 3.9 mA dengan bekalan voltan 2 V.

ACKNOWLEDGEMENTS

I thank all who in one way or another contributed to the completion of this thesis. First, I give thanks to God for protection and ability to do the work.

I would like to express my special appreciation and thanks to my supervisor Dr. Nasri b. Sulaiman, you have been a tremendous mentor for me. I would like to thank you for encouraging my research and for allowing me to grow as a research scientist. Your advice on both research as well as on my career have been priceless. I would like to thank my co-supervisors, Assoc. Prof. Dr. Roslina bt. Mohd. Sidek and Dr. Suhaidi B. Shafie for the patient guidances, encouragements and advices. I also would like to thank all staff members of the Electrical and Electronics Engineering Department at Universiti Putra Malaysia.

A special thanks to my family. Words cannot express how grateful I am to my father, and mother for all of the sacrifices that you've made on my behalf. Your prayer for me was what sustained me thus far. I would also like to thank all of my brother, sister and friends who supported me in writing, and incented me to strive towards my goal.

This thesis was submitted to the Senate of the Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science.

The members of the Supervisory Committee were as follows:

Nasri b. Sulaiman, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Roslina bt. Mohd. Sidek, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Suhaidi b. Shafie, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Member)

BUJANG BIN KIM HUAT, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

Declaration by graduate student

I hereby confirm that:

- this thesis is my original work
- quotations, illustrations and citations have been duly referenced
- the thesis has not been submitted previously or comcurrently for any other degree at any institutions
- intellectual property from the thesis and copyright of thesis are fully-owned by Universiti Putra Malaysia, as according to the Universiti Putra Malaysia (Research) Rules 2012;
- written permission must be owned from supervisor and deputy vice –chancellor (Research and innovation) before thesis is published (in the form of written, printed or in electronic form) including books, journals, modules, proceedings, popular writings, seminar papers, manuscripts, posters, reports, lecture notes, learning modules or any other materials as stated in the Universiti Putra Malaysia (Research) Rules 2012;
- there is no plagiarism or data falsification/fabrication in the thesis, and scholarly integrity is upheld as according to the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2012-2013) and the Universiti Putra Malaysia (Research) Rules 2012. The thesis has undergone plagiarism detection software

Signature: _____ Date: _____

Name and Matric No: Arash Abbasi GS34724

Declaration by Members of Supervisory Committee

This is to confirm that:

- the research conducted and the writing of this thesis was under our supervision;
- supervision responsibilities as stated in the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2012-2013) were adhered to.

Signature: _____
Name of
Chairman of
Supervisory
Committee: _____

Signature: _____
Name of
Member of
Supervisory
Committee: _____

Signature: _____
Name of
Member of
Supervisory
Committee: _____

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

3G	Third-Generation
8-VSB	8-Vestigial Sideband Modulation
ADS	Advance Design System
AT	Auxiliary Transistors
ATSC	Advanced Television Systems Committee
CMOS	Complementary Metal–Oxide–Semiconductor
CS	Common-Source
DSP	Digital Signal Processor
DTV	Digital Television
DVB	Digital Video Broadcasting
FD	Fully-Differential
GPS	Global-Positioning-System
GSM	Global-System-for-Mobile Communications
HRM	Harmonic Rejection Mixer
HRR	Harmonic Rejection Ratio
IIP3	Input-referred Third-Order Intercept Point
IMD3	Third-Order Intermodulation Distortion
LO	Local Oscillator
MGTR	Multiple-Gated-Transistors
MT	Main Transistor
PD	Pseudo-Differential
PTM	Predictive Technology Model
SNR	Signal-to-Noise Ratio
ST	Second Transistor

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Nowadays, the demand for radio frequency (RF) applications such as mobile phones and digital television (DTV) have been increased. Because of this highly request, such development have impassioned several design challenges, especially in simple and highly linear integrated circuit. Mostly, the critical problems in design of RF applications are integration digital base-band with the simple and highly linear front-end circuits [1, 2]. The development of microelectronic circuits had since begun with the innovation of transistors [2, 3] several years ago.

High frequency analog circuits are typically implemented with a GaAs or bipolar device technology, while the base-band digital signal processor (DSP) is implemented within a Complementary metal–oxide–semiconductor (CMOS) technology. However, over the recent years, there has been a vast investigation focusing on the high-frequency analog front-end components, which are designed within the CMOS environment. The suitability and cost effectiveness of CMOS technology for the design and development of digital circuits has helped accelerate the advancement and maturity of this technology [2, 4]. Tremendous advances in CMOS technology have shown no sign of slowing down with current commercially available minimum size channel length of CMOS process of 32 nm by International Business Machines Corporation (IBM), compared to the 2.0 µm technology available in 1983 [4].

With such advancement, effort has been applied in implementing high frequency circuits, especially the analog receiver front-end circuits for radio frequency applications, such as DTV, GSM900, GSM1800, within the CMOS environment [1]. Two of the main issues in the radio frequency applications are high linearity and complexity of design at high frequency operation. The schematic of simple Direct-Conversion receiver is shown in Figure 1-1. There are different blocks in one receiver front-end such as LNA, filters and mixers, and so each of them has the effect on linearity and complexity of design. The designers are looking for ways to design simple and highly linear circuits. The simple but highly linear operation complicates the design of the circuit. Simple circuits have a smaller number of MOSFETs are expected to give a better circuit performance because of small device and stray capacitances but in reality, it works in the opposite way. Therefore, it is highly desirable to design simple and efficient circuits for high linearity [1, 5].

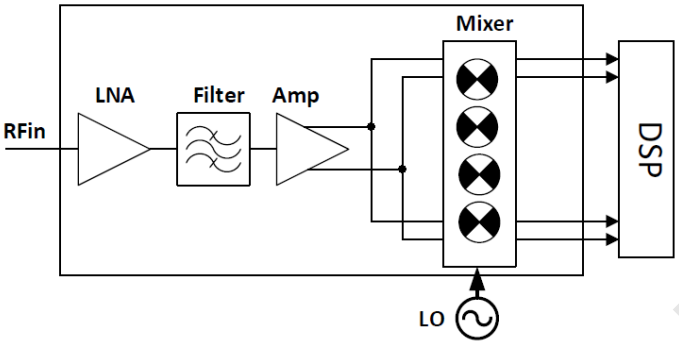

Figure 1-1. Simple Direct-Conversion Receiver Front-End.

In Figure 1-1, the structure of simple Direct-Conversion receiver front-end shows that usually before digital-signal-processing (DSP), some block diagrams such as LNA, filter and mixer are used.

1.2 Significance of LNA and GM-C Filter

In the receiver front-end, LNA is a critical block. Usually, it is employed to extract the extremely low power RF signal from the noise prevalent in the atmosphere. They are used to amplify the RF signal level, without causing significant degradation in the signal-to-noise ratio (SNR), of the received signal. The NF of the LNA, along with the power gain of the low-noise amplifier, primarily determine the NF of the entire receiver, and therefore are critical to the sensitivity of the receiver. Some of the key specifications for low-noise amplifiers are NF, complexity of the design, and linearity [1, 6-8].

In addition, Filters are employed in the RF front-end for a variety of purposes. They are used to limit the spectrum of the transmitted signal [9]. They are also used as image-reject filters in, for example, a direct-conversion receiver [10]. Another requirement for filtering is immediately following the mixing, to eliminate one of the two signals which, in general, result in the output of the mixer (the sum and difference of the RF and LO frequencies) [11].

1.3 Scope of the Study

The focus of this research is on the modification of the MGTR method to reduce the complexity of the design by reducing external biasing circuit. The LNA and third-order Chebyshev filter are introduced with self-biasing MGTR method to increase the linearity. The LNA is modified to use in the receiver front-end of the RF application between frequency ranges of 900-2400 MHz such as GSM900, GSM1800, GSM1900, WCDMA, Bluetooth and GPRS. The third-order Chebyshev filter is modified to prepare the requirements for the direct-conversion receiver front-end for DTV.

1.4 Problem Statements

1.4.1 LNA

The LNA is one of the most critical blocks that determines the sensitivity of the entire receiver. An LNA should have high linearity and low complexity of the design, in order to suppress or minimize the noise contributed by subsequent stages of the receiver. Without the LNA, the low level input signal would be buried by the noise and subsequently the signal-to-noise ratio (SNR) would be further distorted transferring only noise signal to the next stage such as filter or mixer. Hence, not only that LNA should have the low NF which is reported by previous works for RF application bellow 2dB, the linearity performance should be high enough that previous works normally designed IIP3 for RF application between 8 to 13 dB with less complexity of the design which previous LNAs with MGTR topology employed two external biasing voltage that increase complexity of the design and bill-of-material [7, 8, 12].

1.4.2 Third-order Chebyshev Filter

The analog filter is one of the most critical blocks that determines the linearity of the entire receiver. The Filter in direct-conversion receiver for Advanced Television Systems Committee (ATSC) DTV is employed to help mixer to remove undesired signals. Hence, it should have high linearity that previous works normally designed IIP3 for RF application between 15 to 17 dB, low complexity of the design that previous Filters with MGTR topology employed two external biasing voltage that increase complexity of the design and bill-of-material and low noise which is reported by previous works for RF application bellow 16dB, to do not degrade sensitivity of the entire system, with sufficient margin. The third-order Chebyshev filter is consist of first-order RC filter which is linear enough and second-order Gm-C filter. Gm-C filter topology uses transconductor (Gm) block and capacitor (C). The OTA or Gm block is the main building block in the Gm-C filter that the performance of the filter is related to its performance. While several techniques is reported to design it, its major limitations are its poor linearity and complexity of the design [5, 13].

1.5 Objectives

The main goal of this thesis is to modify MGTR method to propose self-biasing MGTR topology. The aim of the self-biasing MGTR topology is to reduce the complexity of the design, bill-of-materials and increase linearity for the LNA and third-order Chebyshev filter.

Hence, in order to achieve all these aims, the objectives of this research are as follows:

- To introduce a self-biasing MGTR method to modify an LNA for high linearity and low complexity of the design.
- To introduce a self-biasing MGTR method to modify an OTA for Gm-C filter for high linearity and low complexity of the design.

The modified self-biasing MGTR method is used to design an LNA and an OTA with 90nm CMOS Predictive Technology Model (PTM) model.

1.6 Thesis Organization

This thesis is organized as follows:

Chapter 2 provides the necessary background discussion about several methods to linearize LNA and OTA. Applications in the range of 900-2400 MHz are introduced. An overview about DTV is provided. Different kinds of Gm-C filter is introduced.

Chapter 3 develops the MGTR method. As a result, self-biasing MGTR is introduced to modify LNA and OTA. NF is calculated for both LNA and third-order Chebyshev filter. The transfer function of third-order Chebyshev filter is calculated. Finally, simulation setup is provided.

Chapter 4 identifies the main performance measures to be analyzed. It summarizes and evaluates the simulation results.

Chapter 5 summarizes the thesis and provides directions for future work.

REFERENCES

[1] Y. Ding and R. Harjani, "High-Linearity CMOS RF Front-End Circuits," 2005.

[2] K.-L. Du and M. N. Swamy, *Wireless communication systems: from RF subsystems to 4G enabling technologies*: Cambridge University Press, 2010.

[3] G.-Q. Zhang, W. van Driel, and X. Fan, *Mechanics of microelectronics* vol. 141: Springer, 2006.

[4] B. Daneshrad and A. M. Eltawil, "Integrated circuit technologies for wireless communications," in *Wireless Multimedia Network Technologies*, ed: Springer, 2002, pp. 227-244.

[5] K. Kwon and K. Lee, "A 23.4 mW 68 dB dynamic range low band CMOS hybrid tracking filter for ATSC digital TV tuner adopting RC and Gm-C topology," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 58, pp. 2346-2354, 2011.

[6] A. Meaamar, B. C. Chye, and Y. K. Seng, "A 3–8 GHz low-noise CMOS amplifier," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 245-247, 2009.

[7] T. H. Jin and T. W. Kim, "A 5.5-mW 9.4-dBm IIP3 1.8-dB NF CMOS LNA Employing Multiple Gated Transistors With Capacitance Desensitization," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 58, pp. 2529-2537, 2010.

[8] T. H. Jin and T. W. Kim, "A 6.75 mw 12.45 dBm IIP3 1.76 dB NF 0.9 GHz CMOS LNA employing multiple gated transistors with bulk-bias control," *Microwave and Wireless Components Letters, IEEE,* vol. 21, pp. 616-618, 2011.

[9] A. Rofougaran, G. Chang, J. J. Rael, J.-C. Chang, M. Rofougaran, P. J. Chang, *et al.*, "A Single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS. I. architecture and transmitter design," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 515-534, 1998.

[10] S. Lerstaveesin, M. Gupta, D. Kang, and B.-S. Song, "A 48–860 MHz CMOS low-IF direct-conversion DTV tuner," *Solid-State Circuits, IEEE Journal of,* vol. 43, pp. 2013-2024, 2008.

[11] L. Anttila, M. Valkama, and M. Renfors, "Circularity-based I/Q imbalance compensation in wideband direct-conversion receivers," *Vehicular Technology, IEEE Transactions on,* vol. 57, pp. 2099-2113, 2008.

[12] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 571-581, 2005.

[13] K. Kwon, H.-T. Kim, and K. Lee, "A 50–300-MHz highly linear and low-noise CMOS filter adopting multiple gated transistors for digital TV tuner

ICs," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 306-313, 2009.

[14] J. Fenk, "Status and prospects of wireless communications," in *Silicon Monolithic Integrated Circuits in RF Systems, 2003. Digest of Papers. 2003 Topical Meeting on*, 2003, pp. 41-44.

[15] G. D, "Mobile WiMAX – Part I: A Technical Overview and Performance Evaluation," august, 2006.

[16] G. D, "Mobile WiMAX – Part II: A Comparative Analysis," May, 2006.

[17] G. J, "IEEE 802.11 standard overview," September, 2007.

[18] W. J.M., "The Next Generation of Wireless LAN Emerges with 802.11n," *Technology at Intel Magazin,* August, 2004.

[19] P. Van Zeijl, J.-W. Eikenbroek, P.-P. Vervoort, S. Setty, J. Tangenherg, G. Shipton, *et al.*, "A Bluetooth radio in 0.18-µm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 1679-1687, 2002.

[20] Y. Wu, S. Hirakawa, U. H. Reimers, and J. Whitaker, "Overview of digital television development worldwide," *Proceedings of the IEEE,* vol. 94, pp. 8-21, 2006.

[21] A. T. S. Committee, "ATSC digital television standard," *Document A/53, Sept,* vol. 16, 1995.

[22] E. N. Committee, "Digital broadcasting systems for television, sound and data services; framing structure, channel coding and modulation for digital terrestrial television," *Norme ETSI, Sophia-Antipolis, France, Doc. pr ETS,* vol. 300, p. 744, 1996.

[23] B. Furht and S. A. Ahson, *Handbook of mobile broadcasting: DVB-H, DMB, ISDB-T, and mediaflo*: CRC Press, 2008.

[24] L. Chen, Y. Wang, C. Wang, J. Wang, C. Shi, X. Weng, *et al.*, "A 4.2 mm 72 mW Multistandard Direct-Conversion DTV Tuner in 65 nm CMOS," 2014.

[25] M. Bouhamame, L. L. Coco, S. Amiot, and S. Toutain, "A 60 dB harmonic rejection mixer for digital terrestrial TV tuner," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 59, pp. 471-478, 2012.

[26] J. R. Tourret, S. Amiot, M. Bernard, M. Bouhamame, C. Caron, O. Crand, *et al.*, "SiP tuner with integrated LC tracking filter for both cable and terrestrial TV reception," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 2809-2821, 2007.

[27] L. Connell, N. Hollenbeck, M. Bushman, D. McCarthy, S. Bergstedt, R. Cieslak, *et al.*, "A cmos broadband tuner IC," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, 2002, pp. 400-476.

[28] I. Mehr, S. Rose, S. Nesterenko, D. Paterson, R. Schreier, H. L'Bahy, *et al.*, "A dual-conversion tuner for multi-standard terrestrial and cable reception," in

VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on, 2005, pp. 340-343.

[29] J.-M. Stevenson, P. Hisayasu, A. Deiss, B. Abesingha, K. Beumer, and J. Esquivel, "A multi-standard analog and digital TV tuner for cable and terrestrial applications," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 210-597.

[30] C.-H. Heng, M. Gupta, S.-H. Lee, D. Kang, and B.-S. Song, "A CMOS TV tuner/demodulator IC with digital image rejection," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2525-2535, 2005.

[31] J. Van Sinderen, F. Seneschal, E. Stikvoort, F. Mounaim, M. Notten, H. Brekelmans, *et al.*, "A 48-860MHz digital cable tuner IC with integrated RF and IF selectivity," in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 2003, pp. 444-506.

[32] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, *et al.*, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 2003-2015, 2001.

[33] H.-K. Cha, S.-S. Song, H.-T. Kim, and K. Lee, "A CMOS harmonic rejection mixer with mismatch calibration circuitry for digital TV tuner applications," *Microwave and Wireless Components Letters, IEEE*, vol. 18, pp. 617-619, 2008.

[34] C.-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim, and S.-G. Lee, "An ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB system," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 544-547, 2005.

[35] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, pp. 1433-1442, 2004.

[36] H.-W. Chiu, S.-S. Lu, and Y.-S. Lin, "A 2.17-dB NF 5-GHz-band monolithic CMOS LNA with 10-mW DC power consumption," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 813-824, 2005.

[37] P. Sivonen and A. Parssinen, "Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 1304-1313, 2005.

[38] Z. Li and R. Quintal, "A dual-band CMOS front-end with two gain modes for wireless LAN applications," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 2069-2073, 2004.

[39] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 2422-2433, 2008.

[40] B. Park, S. Choi, and S. Hong, "A low-noise amplifier with tunable interference rejection for 3.1-to 10.6-GHz UWB systems," *Microwave and Wireless Components Letters, IEEE,* vol. 20, pp. 40-42, 2010.

[41] Y.-L. Wei, S. S. Hsu, and J.-D. Jin, "A low-power low-noise amplifier for K-band applications," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 116-118, 2009.

[42] C. Xin and E. Sanchez-Sinencio, "A linearization technique for RF low noise amplifier," in *Circuits and Systems, 2004. ISCAS'04. Proceedings of the 2004 International Symposium on*, 2004, pp. IV-313-16 Vol. 4.

[43] B. M. Ballweber, R. Gupta, and D. J. Allstot, "A fully integrated 0.5-5.5 GHz CMOS distributed amplifier," *Solid-State Circuits, IEEE Journal of,* vol. 35, pp. 231-239, 2000.

[44] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6-22-GHz broadband CMOS distributed amplifier," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, 2003, pp. 103-106.

[45] T.-Y. Lo and C.-C. Hung, *1V CMOS Gm-C Filters: Design and Applications*: Springer, 2009.

[46] S. Hori, T. Maeda, N. Matsuno, K. Numata, N. Yoshida, Y. Takahashi, *et al.*, "A widely tunable CMOS Gm-C filter with a negative source degeneration resistor transconductor," in *Solid-State Circuits Conference, 2003. ESSCIRC'03. Proceedings of the 29th European*, 2003, pp. 449-452.

[47] A. A. Fayed and M. Ismail, "A low-voltage, highly linear voltage-controlled transconductor," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 52, pp. 831-835, 2005.

[48] D. Morozov and A. Korotkov, "A realization of low-distortion CMOS transconductance amplifier," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 48, pp. 1138-1141, 2001.

[49] G. Bollati, S. Marchese, M. Demicheli, and R. Castello, "An eighth-order CMOS low-pass filter with 30-120 MHz tuning range and programmable boost," *Solid-State Circuits, IEEE Journal of,* vol. 36, pp. 1056-1066, 2001.

[50] S. Dosho, T. Morie, and H. Fujiyama, "A 200-MHz seventh-order equiripple continuous-time filter by design of nonlinearity suppression in 0.25-µm CMOS process," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 559-565, 2002.

[51] J. Silva-Martinez, J. Adut, J. M. Rocha-Perez, M. Robinson, and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 216-225, 2003.

[52] M. Mobarak, M. Onabajo, J. Silva-Martinez, and E. Sanchez-Sinencio, "Attenuation-predistortion linearization of CMOS OTAs with digital correction of process variations in OTA-C filter applications," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 351-367, 2010.

[53] Y. Sun, C.-J. Jeong, I.-Y. Lee, J.-S. Lee, and S.-G. Lee, "A 50-300-MHz low power and high linear active RF tracking filter for digital TV tuner ICs," in *Custom Integrated Circuits Conference (CICC), 2010 IEEE*, 2010, pp. 1-4.

[54] C. Garcia-Alberdi, A. Lopez-Martin, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo, "Tunable Class AB CMOS Gm-C Filter Based on Quasi-Floating Gate Techniques," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 60, pp. 1300-1309, 2013.

[55] S. Hori, N. Matsuno, T. Maeda, and H. Hida, "Low-Power Widely Tunable Gm-C Filter Employing an Adaptive DC-blocking, Triode-Biased MOSFET Transconductor," 2014.

[56] T. W. Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 223-229, 2004.

[57] B. Kim, J.-S. Ko, and K. Lee, "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," *Microwave and Guided Wave Letters, IEEE*, vol. 10, pp. 371-373, 2000.

[58] S. Tanaka, F. Behbahani, and A. Abidi, "A linearization technique for CMOS RF power amplifiers," in *VLSI Circuits, 1997. Digest of Technical Papers., 1997 Symposium on*, 1997, pp. 93-94.

[59] B. Kim, J.-S. Ko, and K. Lee, "Highly linear CMOS RF MMIC amplifier using multiple gated transistors and its Volterra series analysis," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, 2001, pp. 515-518.

[60] T. W. Kim, B. Kim, I. Nam, B. Ko, and K. Lee, "A low-power highly linear cascoded multiple-gated transistor CMOS RF amplifier with 10 dB IP3 improvement," *Microwave and Wireless Components Letters, IEEE*, vol. 13, pp. 205-207, 2003.

[61] B. Razavi and R. Behzad, *RF microelectronics* vol. 1: Prentice Hall New Jersey, 1998.

[62] P. E. Allen, D. R. Holberg, P. E. Allen, and P. Allen, *CMOS analog circuit design*: Holt, Rinehart and Winston New York, 1987.

[63] A. Technologies. Harmonic Balance Simulation [Online]. Available: http://cp.literature.agilent.com/litweb/pdf/rfde2008/pdf/rfdecktsimhb.pdf

[64] A. Technologies. Tuning in Advanced Design System [Online]. Available: http://cp.literature.agilent.com/litweb/pdf/ads2008/optstat/ads2008/Tuning_in_Advanced_Design_System.html

[65] C. T. Group, "dBm convertor."