UNIVERSITI PUTRA MALAYSIA

HIGH ACCURACY DUAL OUTPUT VOLTAGE REFERENCE CIRCUIT FOR DIFFERENTIAL 10-BIT SUCCESSIVE APPROXIMATION REGISTER ANALOG TO DIGITAL CONVERTER USING 180nm TECHNOLOGY

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By

SITI IDZURA BINTI YUSUF

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

May 2020

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DEDICATION

Every challenging work, needs self efforts as well as,

prays of day and night from Ayah and Mak that make me able to get such success and honour,

patiently and tremendously supports from my husband Muhammad Syukur, throughout these stressful years,

and finally, to Sara, Tina, Dira and Rina for being wonderful and colourful journey of my life.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Doctor of Philosophy

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May 2020

Chairman : Associate Professor Suhaidi Shafie, PhD
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Voltage reference circuit produces reference voltage that is independent of fabrication process, temperature and supply voltage (PVT) variation. Differential successive approximation register (SAR) analog to digital converter (ADC) that converts an analog signal to digital signal is very much dependent on accurate reference voltage which defines the resolution of the converter. It requires two reference voltages namely V_{REF} and V_{CM}. V_{REF} is used to set the full-scale voltage range while the common-mode voltage, V_{CM} defines an initial value of most significant bit (MSB) digital output. V_{CM} is designed as such that it is half of V_{REF} and independent of process, voltage and temperature (PVT) variations. The deviation of the V_{CM} develops an offset that shifts the transfer function of the ADC. Consequently, it reduces the dynamic range of the analog input to be digitised. The evolution of technology has favoured in a system on chip integration of the voltage reference and SAR ADC because it reduces design circuit area and consumes less power. However, based on the previous literatures, the impact of voltage reference circuits integrated with SAR ADC on a single die has not been discussed in depth. Hence, this thesis features the design and implementation of a high accuracy dynamic dual output voltage reference circuit for a 200kS/s differential 10-bit SAR ADC using a Silterra 0.18µm process with a supply voltage of 1.8V on a common die. The measurement of the fabricated chips is able to generate constant reference voltages for the V_{REF} is that 1.2V±0.03V. Meanwhile, the V_{CM} deviates as much as ±4mV between temperatures ranging from 0^0C and 80^0C across ±10% voltage supply variation. The measurement result shows that the circuit have sufficient drive capability to provide dual reference voltages to the SAR ADC. The voltage reference circuit achieves a good performance on the SAR ADC with 0.4LSB differential nonlinearity (DNL), 57.39dB Signal-to-noise and distortion ratio (SINAD) and an effective number of bits (ENOB) of 9.5 bits. The

voltage reference circuit functions accurately in temperature sensor application between 0^0C and 80^0C temperature input range.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

LITAR RUJUKAN VOLTAN DUA KELUARAN BERKEJITUAN TINGGI UNTUK PEMBEZAAN 10-BIT PENGUBAH ANALOG KEPADA DIGITAL JENIS SAR MENGGUNAKAN TEKNOLOGI 180nm

Oleh

SITI IDZURA BINTI YUSUF

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Fakulti : Kejuruteraan

Litar rujukan voltan menghasilkan voltan rujukan yang bebas daripada perubahan proses fabrikasi, suhu dan voltan. Penukar isyarat analog kepada digital jenis SAR sangat bergantung kepada voltan rujukan untuk menentukan resolusi penukar. Penukar SAR memerlukan dua voltan rujukan iaitu V_{REF} dan V_{CM}. V_{REF} digunakan untuk menetapkan julat voltan berskala penuh manakala V_{CM} menetapkan nilai permulaan bit. Nilai V_{CM} direka untuk menjadi separuh daripada V_{REF} dan bebas daripada perubahan proses, voltan dan suhu. Penyimpangan V_{CM} akan mengakibatkan satu *offset* yang menyebabkan pemindahan fungsi ADC teranjak. Oleh sebab itu, ia mengurangkan isyarat analog untuk didigitalkan. Evolusi teknologi litar rujukan voltan dan penukar analog kepada digital menjurus kepada pembangunan sistem pada satu cip kerana ianya dapat mengurangkan keluasan pembangunan litar dan menjimatkan tenaga. Walau bagaimanapun, berdasarkan kepada karya terdahulu, kesan rujukan voltan yang disepadukan dengan Penukar SAR pada satu cip tidak dibincangkan secara mendalam. Oleh itu, tujuan tesis ini adalah untuk mereka bentuk litar rujukan voltan yang menghasilkan dua output berketepatan tinggi yang akan digabungkan dengan Penukar 10-bit perbezaan SAR berkelajuan 200kS/s menggunakan teknologi Silterra 0.18µm CMOS dengan voltan bekalan 1.8V. Pengukuran terhadap cip yang difabrikasi mampu menghasilkan voltan rujukan tetap untuk V_{REF} ialah 1.2V±0.03V. Manakala V_{CM} menyimpang sebanyak $V_{REF}/2$ ±4mV pada julat suhu antara 0^0C dan 80^0C dan ±10% perubahan voltan bekalan . Litar ini mempunyai keupayaan memandu yang mencukupi untuk menyediakan voltan rujukan kepada Penukar SAR. Hasil pengukuran mencapai prestasi yang baik terhadap Penukar SAR dengan 0.4LSB perbezaan linear, kadar terhadap hingar dan gangguan telah berlaku sebanyak 57.39dB dan bilangan bit yang berkesan adalah sebanyak 9.5 bit. Litar rujukan voltan ini juga berfungsi dengan baik dalam aplikasi pengesan suhu antara julat suhu 0^0C hingga 80^0C.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

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Date: 10 September 2020

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog Digital Converter
BGR	Bandgap Reference
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary to Absolute Temperature
DAC	Digital to Analog Converter
DC	Direct Current
DEC	Decimal
DNL	Differential Nonlinearity
DRC	Design Rules Check
DUT	Device Under Test
EDA	Electronic Design Automation
ENOB	Effective Number of Bit
EOC	End of Conversion
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistor
FFT	Fast Fourier Transform
FSR	Full Scale Range
FVF	Flip Voltage Follower
GM	Gain Margin
GND	Ground
IC	Integrated Circuit
INL	Integration Nonlinearity
I/O	Input/Output

IoT	Internet of Thing
LDO	Low Dropout Oscillator
LSB	List Significant Bit
LVS	Layout Versus Schematic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPW	Multi Project Wafer
MSB	Most Significant Bit
NMOS	N-type Metal Oxide Semiconductor
OpAmp	Operational Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
PMOS	P-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage and Temperature
QFN	Quad Flat No-leads
RC	Resistance-capacitance
RF	Radio Frequency
RVBuffer	Reference Voltage Buffer
SAR	Successive Approximation Register
SINAD	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
TC	Temperature Coefficient
THD	Total Harmonic Distortion
UGF	Unity Gain Frequency
VCTAT	Voltage Complementary to Absolute Temperature
VPTAT	Voltage Proportionate to Absolute Temperature

LIST OF SYMBOLS

δV_{IN}	AC voltage input
δV_{OUT}	AC voltage output
η	curvature coefficient
μ_n	Electron mobility
^0C	celcius
C	process-dependent constant
C_{O1}	Output capacitor for V_{REF}
C_{O2}	Output capacitor for V_{CM}
C_{OX}	Oxide capacitance
EN	Enable input
fP_{VCM}	Frequency pole of V_{CM}
fP_{VREF}	Frequency pole of V_{REF}
fZ_{LOAD}	Frequency zero load
d	Distortion factor
K	Resistor ratio
k	Boltzman constant
I	Current
I_D	Drain current
I_{NM}	Negative Input
I_{NP}	Positive Input
I_S	Saturation current
I_{SD}	Source-drain current
L	Length of the channel in field-effect transistors
N	No. of bit
P	Power
Ppm	parts per million
Q	Electron charge
R_{pass}	PMOS pass transistor
T	Temperature
T_0	Absolute temperature

T_{MAX}		Maximum Temperature
T_{MIN}		Minimum Temperature
V		Voltage
V_{BE}		Base Emitter Voltage
V_{CM}		Common-mode Voltage
V_D		Voltage across diode
V_{DDA}		Voltage Supply
V_{DO}		Dropout Voltage
V_G		Gate Voltage
V_{GS}		Gate Source Voltage
V_{IN}		Voltage Input
V_{REF}		Reference Voltage
V_{REFL}		Low Reference Voltage
V_{REFMAX}		Maximum Reference Voltage
V_{REFMIN}		Minimum Reference Voltage
V_{RMS}		Root mean square voltage
V_T		Thermal Voltage
V_{TH}		Threshold Voltage
W		Width of the channel in field-effect transistors
ΔV_{IN}	-	Varying supply voltage
ΔV_{REF}		Reference voltage variation
$\Delta\varphi$		Phase difference

CHAPTER 1

INTRODUCTION

This chapter introduces to the readers to the framework of this research. An operation of voltage reference for differential Successive Approximation Register Analog Digital Converter (SAR ADC) architecture is presented. The literature of existing design of voltage reference is also reviewed, which explains the research motivation from which the drawback was identified. Subsequently, the objectives are defined as a guide to achieve the research goal within the scope of the study, and the chapter concludes with the thesis's organization.

1.1 Research Background

The latest technology advancement has provided an opportunity for people to use the Internet of Thing (IoT). This new IoT invention is mostly implemented in a single system-on-chip (SoC) to provide the highest level of integration and conservation of the design area. The voltage reference is a necessary part of the power management system to provide a constant voltage that is insensitive to the fabrication process, supply voltage and temperature (PVT). It is commonly used as a reference for various amplifiers, comparators, data converters and many other analogs and mixed-signal functions.

The reference voltage sets the limit of the ADC input range. It is basically the benchmark against which every proportion of analog input correspondes to the digital code. Also, the reference voltage defines the resolution of the ADC by dividing the reference voltage value by the total of conversion code. In establishing the requirement of ADC system performance, each component in the system probably will have an associated error. One of the main potential sources of errors in an ADC is the reference voltage (Siva & Chakravarty, 2015). Thus, the goal of voltage reference circuit is designed to keep the error under an acceptable limit. Any disturbance at the reference voltage contributes to the output code that causes the limitation of the ADC performance (Walsh, 2013).

Analog-to-Digital Converter (ADC) is a device to represent the quantity of analog signals being measured and subsequently translates it into digital form. Currently, ADC offers high-performance signal conversion for a wide range of application requirements. Four main types of ADCs are usually used which are subjected to their desired applications, namely flash, pipelined, delta-sigma ($\Sigma\Delta$) and successive approximation register (SAR).

Flash converter offers the fastest rate of conversion that could reach a maximum speed of 5 GS/s but has low resolution which is lesser than 8-bit among others (Inamdar, Sahu, Ren, & Setoodeh, 2015)(Jeon, Yoo, Kim, & Yoo, 2017). It is designed for a

wide bandwidth of applications such as satellite communication. The pipelined converter is designed for high resolution up to 16-bit and retains the sampling rate greater than 50 MSPS (C. Wu & Yuan, 2019)(Moon, Jo, Kim, Choi, & Ko, 2019), and it is suitable for digital video and medical imaging. Meanwhile, ΣΔ converter employs a very high resolution of 12-24 bits but with lower sampling speed of 15 KS/s (Mehrjoo, Taherzadeh-sani, & Nabki, 2016)(Pini, 2018). It is mostly used in high precision converter applications such as automation test equipment.

Challenges still persist for designers to balance the requirements for performance, device complexity and size. SAR ADC architecture is extensively used in low power and medium speed from 10KS/S to 10MS/s. It provides an excellent combination between resolution to 18 bits, die area, and circuit complexity compared to other ADC (Zahrai & Onabajo, 2018)(H. Wei et al., 2012)(Ku, Xu, Kuan, Wang, & Frank, 2012). The SAR ADC uses a binary search algorithm to convert an analog signal to a digital form. The fundamental architecture of SAR ADC is shown in Figure 1.1.

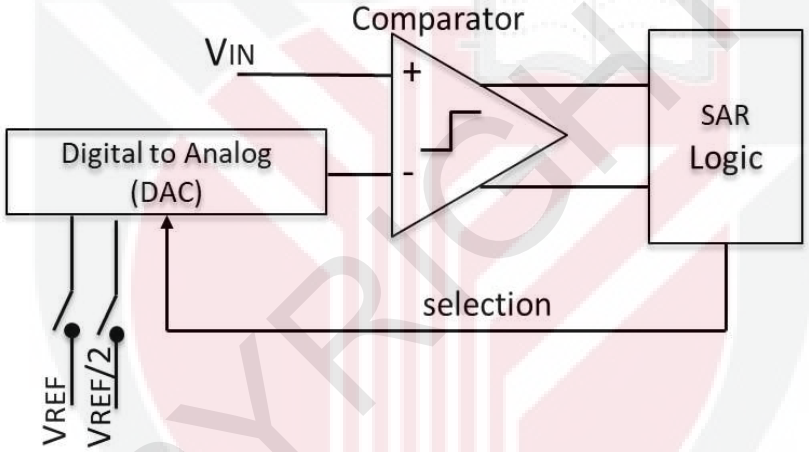

Figure 1.1 : Basic architecture of SAR ADC
(Xingyuan, Jianming, Zhangming, & Yintang, 2010)

A full-scale range voltage (V_{REF}) of the analog input signal is determined by the reference voltage of the ADC. The binary search algorithm is implemented by setting the midscale value of the most significant bit (MSB) that is equal to one. It needs to be set to the digital-to-analog converter (DAC) capacitance switch at $V_{REF}/2$. The output of the ADC is determined by the approximate value that is performed by the comparator.

The counting sequence of the binary search algorithm for 3-bit conversion is expressed in Figure 1.2. Initially, the midscale value sets a high MSB value (100). This digital output is converted to an analog value by DAC that produces V_{DAC}. The next bit is determined by a V_{DAC} of either ¾ V_{REF} or ¼ V_{REF}. Then, the V_{DAC} is compared with the voltage sample input V_{IN}. If the V_{IN} is greater than V_{DAC}, it gives a positive difference of comparator output; the next bit of MSB value becomes high (110).

Conversely, if V_{IN} is less than V_{DAC}, the comparator output delivers a logic low value. This condition resets the MSB value to logic 0 (000). The SAR control logic then sets the next bit to be high (110) and second comparison is made. Since V_{IN} is less than V_{DAC}, bit 1 is set to 0. The DAC is then set to 101, and the final comparison is performed. Subsequently, V_{IN} greater than V_{DAC} bit 0 remains at 1.

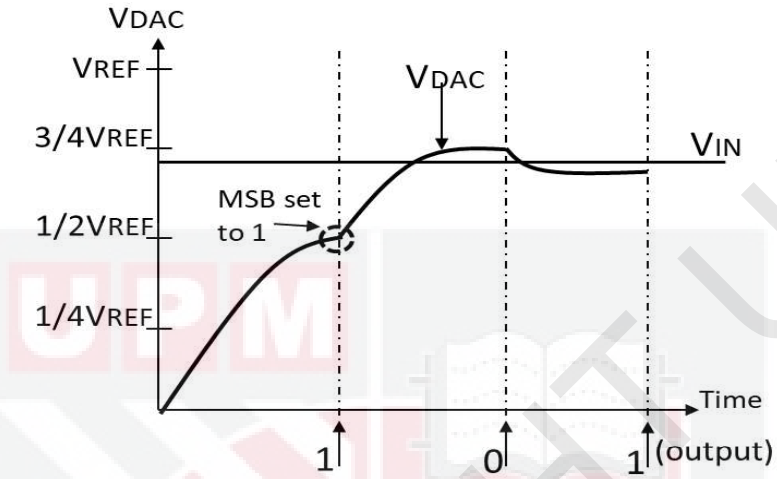

Figure 1.2 : Binary search algorithm of a 3-bit SAR ADC

Since the SAR ADC is highly dependent to the reference voltage, a voltage reference circuit must designed to generate highly accurate reference voltage that is able to fulfill the SAR ADC requirement.

1.2 Research Problem

Accurate conversion of SAR ADC relies on the accuracy of the voltage references because the comparison between an analog input voltage and a reference voltage creates the conversion code values (Siva & Chakravarty, 2015). Differential SAR ADC architecture requires dual reference voltages to digitise the analog input voltage. The V_{REF} sets the full-scale range analog input while the V_{CM} sets the initial MSB value of the conversion. Since the V_{CM} sets the initial MSB value of digital output, it must be continuously designed to remain at half of V_{REF} over the fabrication process and every change of temperature and supply voltage during the circuit operation. Otherwise, it develops an ADC offset and reduces the dynamic range of the analog input voltage of the converter as shown in Figure 1.3. Consequently, it causes the digital output value to saturate before the analog input voltage reaches maximum value.

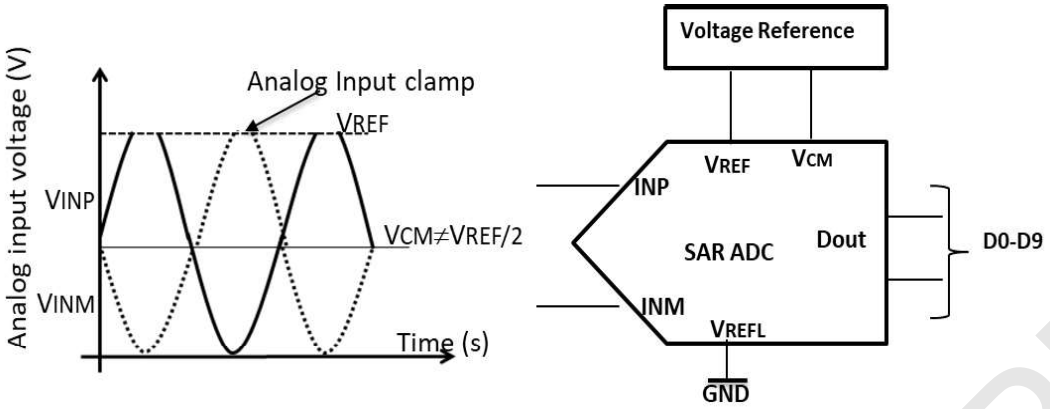

Figure 1.3 : Fully differential 10-bit SAR ADC system architecture

Since the voltage reference accuracy influences the SAR ADC performance, the SAR ADC integrates with an external monolithic voltage reference device due to the output that can be adjusted to the desired voltage (C. C. Liu, Chang, Huang, & Lin, 2010)(Song, Xue, Xie, Fan, & Geng, 2016)(Song, Y., Xue, Z., Xie, Y., Fan, S. and Geng, 2016)(Shim et al., 2017). However, the technology has evolved towards the integration of system on chip (SoC) because it consumes less power and reduces circuit area than multi-chip circuit with similar functionality. Thus, the integrated chip is on high demand for currently available applications.

Drive capability is another concern in integrating a voltage reference with SAR ADC. The primary source of error that degrades the performance of SAR ADC comes from the unstable reference voltage. The undershooting and overshooting of reference voltages that deviate more than 1LSB produce an error of digital outputs. The inadequate drive strength of current voltage reference circuit causes switching transients of the DAC's ADC during the conversion process which is observed as errors in conversion .The measurement results in (Huang, Ting, & Chang, 2016) explain the effect of the undershoot voltage reference that contributes to the "missing code" of the digital output. Hence, the voltage reference circuit must be able to drive sufficient current to maintain the reference voltage from drooping significantly throughout the conversion (Walsh, 2013).

Based on previous literature, most of the designers optimise the performance of voltage reference and differential SAR ADC independently (Dancy, Amirtharajah, & Chandrakasan, 2000)(Shrivastava, Craig, Roberts, Wentzloff, & Calhoun, 2015)(Song et al., 2016)(I. Lee, Sylvester, & Blaauw, 2017)(Berens, Mai, Feddeler, & Pietri, 2019). It is observed that the impact of the voltage reference accuracy to ADC performance is not investigated in depth. Although there are on-chips that are designed with the voltage reference integrated into the SAR ADC, these designs require high supply voltage to activate the chip (Instruments, 2017)(Maxim, 2018).

The ADC requires high accuracy reference to digitise temperature input in temperature sensor application. The sensing element produces an analog voltage with every

temperature change and this voltage takes a ratio of reference voltage before converting into digital output. Consequently, unstable reference circuit causes an error code of digital output. Thus, the performance of voltage reference is investigated in depth in temperature sensor application.

In order to produce a robust voltage reference design, it has to pass through 45 corners simulation process, voltage and temperature (PVT) variation and Monte Carlo analysis. It aims to hinge on a high yield production by taking into consideration the corners that are appropriate and the ones that are not.

Therefore, with all above mentioned issues, an integration of the voltage reference circuit with SAR ADC on a single chip is proposed to provide advantages of increasing the accuracy and drive capability reference voltage for the differential SAR ADC.

1.3 Research Objectives

This research aims to achieve a high accuracy dual output voltage reference of V_{REF} is 1.2V±0.03V and V_{CM} is $V_{REF}/2$ ±15mV across PVT variation. In order to achieve the aim of the research, three research objectives have been set as follows:

1. To design and characterise a new voltage reference circuit that produces an accurate dual reference voltage for differential SAR ADC.
2. To evaluate voltage reference functionality and drive capability by integrating it with differential SAR ADC.
3. To validate the performance of voltage reference in the real utilisation of temperature sensor application.

1.4 Research Scope and Limitation

This research focuses on the design of a voltage reference circuit and test the fabricated chips to obtain high accuracy of circuit performance. The circuit is to be designed using the BSIM model transistor 0.18µm CMOS technology provided by Silterra technology. The schematic is designed, and the parameters is simulated using Cadence tools software. The parameters consist of initial error, line regulation temperature drift, stability and drive capability. The post layout is simulated across 45 corners PVT variation between temperature range -40^{0}C and 125^{0}C. However, the temperature test is measured ranging from 0^{0}C to 80^{0}C only. The test cannot be conducted at the highest temperature up to 125^{0}C because some of the devices on the test board are working at a maximum temperature of ±90^{0}C. In addition, for low-temperature tests down to -40^{0}C, the limitation of liquid nitrogen supply is a caused factor.

Moreover, the PSRR performance is tested on post layout simulation only because the measurement equipment with a careful setup should be prepared to obtain a significant

and accurate PSRR result (Rice & Sandler, 2013). The equipment is the tool that is able to correctly mix DC and AC input signals to avoid the output signal from being attenuated. Picotest J2120A Line Injector is a recommended tool for signal mixing to produce an accurate PSRR measurement.

The circuit generated dual reference voltage outputs, V_{REF} is 1.2V ±0.03V and V_{CM} is $V_{REF}/2$±15mV, to fulfil the requirement of the 10-bit differential SAR ADC's reference voltage that was designed by the IC design department team, MIMOS Berhad. The functionality and drive capability of the voltage reference circuit is measured by integrating it with SAR ADC. The circuit is also tested in a temperature sensor application to verify the functionality. The parameters of the fabricated chips are tested using the custom test board and other test bench equipment provided by MIMOS Berhad.

This work is part of a collaboration between Universiti Putra Malaysia and IC design department team, MIMOS Berhad. The SAR ADC circuit design and the source code for testing the ADC performance remain confidential.

1.5 Organization of the Thesis

This thesis is arranged into seven chapters. Following this introductory chapter is Chapter 2, which defines crucial parameters that should be taken into consideration when designing a voltage reference in a fully differential SAR ADC application. A topology of voltage reference circuit is reviewed. The chapter ends with highlighting the significance of the research work in relation to the findings of previous research.

Chapter 3 explains the full description of the voltage reference circuit design. The schematic, simulated parameter and layout formation of the proposed circuit is presented. The measurement setup for the fabricated chip is also presented.

Chapter 4 presents a comparison of the post-layout simulation and measurement results. The results analyses the voltage reference accuracy including the parameters of the initial error, line regulation, temperature drift, stability, and power consumption.

Chapter 5 evaluates the functionality and drive capability of the voltage reference circuit by integrating with the SAR ADC. The SAR ADC performance of the static and dynamic parameters is analysed. The result is then compared with monolithic voltage reference chip.

Chapter 6 describes the performance of the voltage reference circuit in a temperature sensor application. The measurement result of temperature to digital value is obtained. The thesis is concluded in Chapter 7. It summarises and concludes the research work. Several suggestions related to future works are also proposed.

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LIST OF PUBLICATIONS

Journals

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(Best paper Award)

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