QUIESCENT CURRENT REDUCTION OF SELF-COMPENSATED LOW-DROPOUT VOLTAGE REGULATOR

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By

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QUIESCENT CURRENT REDUCTION OF SELF-COMPENSATED LOW-DROPOUT VOLTAGE REGULATOR

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October 2019

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Low-Dropout Voltage Regulator (LDO) is a linear regulator which is mainly used to regulate noiseless supply voltage for analog and Radio Frequency (RF) circuits. Today, the shrinking of transistor size due to the advancement of process technology and the increasing interests in the Internet-of-Thing (IoT) have increased the market demand for portable, wearable and implantable electronic devices. This has driven the need for low power Silicon-on-Chip (SoC) design which includes the integration of LDO into SoC.

Analog and RF circuits have contributed to significantly high percentage of current consumption in low power SoC designs, mainly during stand-by mode. The reduction of quiescent current in analog LDO circuits become very important in order to reduce power consumption and to improve the efficiency of LDO especially during low output load current. Quiescent current is the current needed to keep LDO's internal circuit in vigilant. However, with the absent of large off-chip compensation-capacitor for LDO in SoC, an excessive current is required to maintain ac loop stability of LDO system, especially during low output load current condition.

A self-adjustable current reduction circuit technique has been proposed in this thesis to reduce this unnecessary current when output load current increases from zero value. On top of that, a self-compensation circuit technique is also been proposed to cater the worst case loop stability issue when load current reducing to zero. In this technique, the UGF has been shifted to a lower frequency away from the second pole frequency according to the amount of output load current. It is done using a current feedback circuit, where the total gain is lowered without affecting the location of dominant pole. The self-compensation technique further reduces the total quiescent current, and avoid the excessive current to be used to keep the second pole at higher frequency.

The proposed LDO has been designed and fabricated using 0.13μm CMOS process technology. The results has shown that the proposed LDO exhibits good stability with phase margin more than 60° for all output load condition. The LDO's total quiescent current is only 7.4μA at zero output load current, and 17.7μA at maximum output load current of 100mA. The total quiescent current measurement result on LDO with BGR circuit is 33.1μA, where the BGR consumed 20μA. This LDO is functional at 1.20V supply voltage with 200mV dropout voltage.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PENURUNAN ARUS SENYAP PENGATUR VOLTAN PERBEZAAN KELUARAN RENDAH PAMPASAN DIRI

Oleh

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Pengatur voltan perbezaan keluaran rendah (LDO) adalah sejenis pengatur linear yang digunakan terutamanya untuk mengawal voltan bekalan tanpa hingar untuk litar analog dan Radio Frekuensi (RF). Hari ini, pengurangan saiz transistor yang disebabkan oleh kemajuan teknologi proses peningkatan minat dalam *Internet-of-Thing* (IoT) telah meningkatkan permintaan pasaran untuk alat elektronik yang mudah alih, boleh pakai dan boleh implan. Ini telah mendorong keperluan reka bentuk *Silicon-on-Chip* (SoC) kuasa rendah yang merangkumi integrasi LDO ke dalam SoC.

Litar Analog dan RF menyumbang kepada peratusan penggunaan arus yang ketara di dalam reka bentuk SoC kuasa rendah, terutamanya semasa mod *standby*. Pengurangan arus senyap dalam litar analog LDO menjadi sangat penting untuk mengurangkan penggunaan kuasa dan untuk meningkatkan kecekapan LDO terutama semasa arus beban keluaran adalah sangat rendah. Arus senyap adalah arus yang diperlukan untuk memastikan litar dalaman LDO dalam keadaan waspada. Walaubagaimanapun, dengan ketiadaan kapasitor pampasan luar cip yang besar untuk LDO di SoC, arus yang berlebihan diperlukan untuk mengekalkan kestabilan gelung ac sistem LDO, terutamanya pada keadaan arus beban keluaran rendah.

Teknik litar pengurangan arus laras diri telah dicadangkan dalam tesis ini untuk mengurangkan arus yang tidak perlu semasa arus beban meningkat daripada nilai sifar. Di samping itu, teknik litar pampasan diri juga telah dicadangkan untuk menyelesaikan masalah kestabilan gelung terburuk apabila arus beban berkurangkan menjadi sifar. Dalam teknik ini, frekuensi gandaan-uniti (UGF) telah beralih kepada frekuensi yang lebih rendah jauh dari frekuensi tiang kedua mengikut jumlah arus beban keluaran. Ia dilakukan menggunakan arus suap balik di mana jumlah gandaan diturunkan tanpa menjejaskan lokasi tiang dominan. Teknik pampasan diri akan terus mengurangkan jumlah arus senyap, dan mengelakkan arus yang berlebihan untuk digunakan untuk menahan tiang kedua dalam frekuensi yang lebih tinggi.

LDO yang dicadangkan telah direka dan difabrikasi menggunakan teknologi proses CMOS 0.13µm. Hasilnya menunjukkan bahawa LDO yang dicadangkan menunjukkan kestabilan yang baik dengan margin fasa lebih daripada 60° untuk semua keadaan beban keluaran. Arus dalaman LDO hanya 7.4µA pada arus beban sifar, dan 17.7µA pada arus keluaran maksimum 100mA. Jumlah hasil pengukuran arus senyap pada LDO bersama litar *bandgap reference* (BGR) adalah 33.1µA, dimana BGR menggunakan 20µA. LDO ini berfungsi pada voltan bekalan 1.20V dengan voltan perbezaan keluaran sebanyak 200mV.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

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LIST OF ABBREVIATIONS

BGR	Bandgap Reference
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary to Absolute Temperature
EA	Error amplifier
Gm	Transconductance
G_{ND}	Ground
IC	Integrated Circuit
IoT	Internet-of-Thing
LDO	Low-Dropout Regulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel MOSFET
OTA	Operational Transconductance Amplifier
p_{-3dB}	Dominant pole
PMOS	P-Channel MOSFET
PNP	P-type Bipolar Junction Transistor
PTAT	Proportional to Absolute Temperature
PVT	Process-Voltage-Temperature
SAC	Sensing and Control Circuit
SoC	System on Chip
TC	Temperature Coefficient
UGF	Unity Gain Frequency
V_{DD}	Voltage Drain Drain
V_{DS}	Drain-Source voltage
V_{DSAT}	Saturation Drain-Source voltage
V_{EB}	Emitter-Base voltage
V_{GS}	Gate-Source voltage
V_{SD}	Source-Drain voltage
V_{SDSAT}	Saturation Source-Drain voltage
V_{SG}	Source-Gate voltage
V_{TH}	Threshold voltage

CHAPTER 1

INTRODUCTION

1.1 An overview of LDO in Silicon-on-Chip (SoC)

In recent years, the market demand for portable and wearable electronic devices have been driven by the technology revolution trend such as Internet-of-Thing (IoT) and biomedical engineering. The IoT trend has enabled the possibility of many household electrical appliances and portable electronic devices to be connected through internet cloud (Zarate-Roldan, Carreon-Bautista, Costilla-Reyes, & Sanchez-Sinencio, 2015; Koay & Chan, 2017). The wireless communication integrated circuit (IC) devices such as the Radio Frequency integrated circuits (RF ICs) may need standalone power source and the devices itself are required to be low power consumption (Zeng & Tan, 2016). On biomedical technology trend, a convenient portable and wearable devices which is normally used for all hour wireless monitoring on the medical condition of patients are demanding (Goldstein, Kim, Xu, Vanderlick, & Culurciello, 2012; L. Y. Wang, Li, & Wu, 2012; Elzeftawi & Theogarajan, 2013). Long hour operation sustainability devices can be realized with low power consumption chips set and low count number of on board components which consume higher current. With the advancement of today's nanotechnology and Micro-Electro-Mechanical Systems (MEMS) technology, the implantable IC has come into reality (Ramos, Ausin, Duque-Carrillo, & Torelli, 2011; Zou & Larsen, 2011; Kok, Huang, Zhu, Siek, & Lim, 2012; Jalalifar & Byun, 2013). In order not to generate any harmful heat on the patients' body, a very low power operational implantable IC chips are therefore required (S.-Y. Lee, Yang, Hsieh, & Fang, 2010; Narasimhan, Chiel, & Bhunia, 2011; Lotfi Navaii, Jalali, & Sadjedi, 2012). All these demands have driven the design trend of low power consumption IC. Furthermore, the shrinking of transistor size in advance process technology nowadays has enabled the full functional circuitry system to be built on a single chip, namely System on Chip (SoC). The SoC methodology not only improved the performance of the circuitry, it has also reduced the number of off-chip components, hence reduces the overall power consumption and cost (W.-M. Chen et al., 2014; L. M. Chen et al., 2015). By and large, these technology trends have further enhanced the demand on low power consumption IC chips with SoC methodology. On the end consumers' point of concern, low power SoC trend is the main factor where the electronic gadgets nowadays are able to sustain longer hours of operation (Y. Park & Salman, 2016).

Low dropout linear regulator (LDO) is one of the most important unit of the power management module (Paul et al., 2016). LDO is usually used to regulate analog or RF circuit modules. Before the trend of SoC taken place, LDO was designed in a single module. The structure of a conventional LDO configuration is shown in Figure 1.1 (Gjanci & Chowdhury, 2011; Márquez et al., 2017). An error amplifier (EA) is used to drive the power transistor. An off-chip capacitor that connected to the output of LDO which comes with its equivalent series resistance (ESR) is used for loop stability compensation of the LDO. With the large capacitance value of the passive component capacitor, the loop stability of LDO module can be easily achieved.

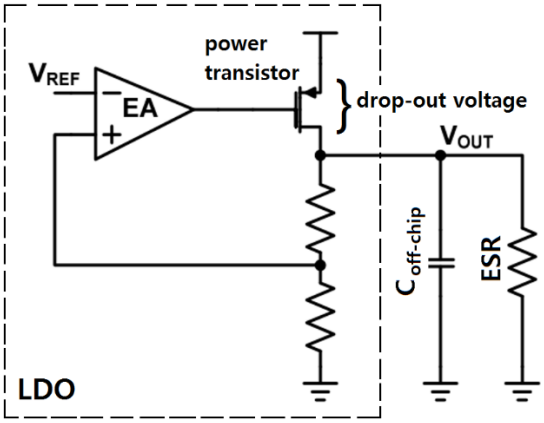

Figure 1.1: Structure of a conventional LDO

In today's low power environment IC chips, power management unit is integrated in a single SoC. The off-chip capacitor is removed and the LDO is integrated into the SoC. However, implementing a large capacitor in silicon will need a very high silicon cost. Therefore, this has created a problematic issue for LDO stability compensation. As such, the dominant pole of LDO has also been shifted to internal circuitry of LDO from its output node (C.-J. Park, Onabajo, & Silva-Martinez, 2014). For low power SoC design, the supply voltage source has decreased to 1.20V or lower for deep submicron process technology smaller than 0.13μm. Whereby the drop-out voltage of power PMOS transistor hasn't been reduced much due to the constraint of the process technology which comes from the source-drain resistance, namely R_{ON} of the power transistor (W.-C. Chen et al., 2014). Drop-out voltage is the voltage drop across the source-drain terminal of the large power PMOS transistor as shown in Figure 1.1. The drop-out voltage becomes relatively higher compare with the supply voltage, thus impact the efficiency of LDO (Avalur & Azeemuddin, 2016; Das et al., 2017). In order to increase the efficiency of the low power LDO, there are research efforts being done to reduce the total quiescent current.

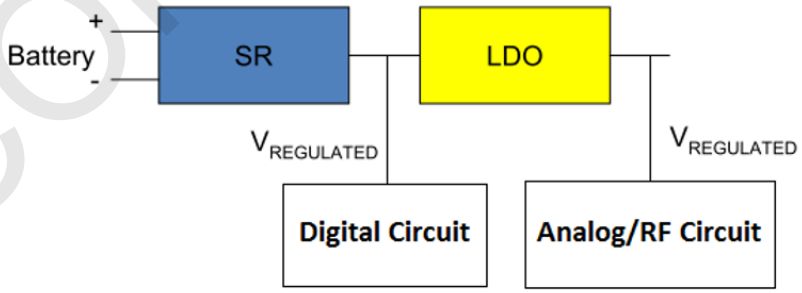

Figure 1.2: Configuration of power management unit in SoC

Figure 1.2 shows the configuration of power management unit in SoC (E. N. Y. Ho & Mok, 2011). The unregulated input supply source to the whole power management unit is normally full of noise signals. The switching regulator, such as DC/DC converter, regulates the supply source for the digital circuitry which is normally a very large circuit. The efficiency of switching regulator is usually very high and able to reach more than 98% (Y. Okuma et al., 2010). But however, switching regulator is not suitable to regulate analog or RF circuitry due to its high switching noise. As shown in Figure 1.2, the LDO input is sourced from the regulated output of switching regulator, and LDO output supplies a clean regulated output to the sensitive analog and RF circuitries. The LDO output is almost noiseless because it has gone through two stages of regulation.

1.2 Motivation

From the statistical analysis, it is known that the majority operation time of most electronic devices are in idle mode (Luders et al., 2011). In order to effectively prolong the sustainability of battery life, it is critical to reduce the power consumption, especially during idle mode operation of the electronic devices (Paul et al., 2016). Analog circuits such as LDO that needs a constant drawing of current from battery will definitely contribute to the draining of battery. To be exact, LDO that regulates all analog and RF circuits are needed in large numbers, thus LDO has become the main culprit in draining the battery during devices idle mode. Hence the reduction of quiescent current in LDO is vital in today low power portable electronic devices (Kubendran et al., 2011; Saint-Laurent et al., 2015). The reduction of quiescent current could further improve the efficiency of the LDO especially during idle state, where the output loading current is zero or very small (Pathak, Hajkazemi, Tavana, Homayoun, & Savidis, 2016). Therefore, designing a low power LDO with low quiescent current is the first motivation of this research work.

Furthermore, stability compensation of SoC integrated LDO during low load current condition has always been a problematic issue. While the load current reducing to low level, the loop stability will continue worsen and probably collapse at the zero load current. More current is usually needed to sustain the stability compensation of the LDO when output load current is reducing (Z. Peng, Lv, & She, 2012). But the increased of quiescent current will worsen the efficiency. Hence another motivation in this research work is to take the challenge in designing a LDO circuit that is able to perform self-compensation by its own, depending on the amount of load current, but at the same time preventing the usage or any increment of quiescent current. To perform both challenges as above which contradict each other is indeed not a direct and easy task.

The scope of this research work mainly focus on the loop stability and the reduction of quiescent current of the LDO during its load current is very low. The limitation is it compromises on other performance of the LDO which involve higher consumption of current such as transient response and slew-rate.

1.3 Problem statements

Figure 1.3 shows the LDO design for SoC application. The voltage reference, V_{REF} is provided by a bandgap reference (BGR). However the low power environment SoC requirement with lower supply voltage which as low as 1.20V has made conventional 1.12V output voltage of BGR not viable anymore (Jang, Park, Jeong, & Cho, 2016).

Figure 1.3 shows no external off-chip capacitor. C_L represents the load capacitance. The SoC requirement have put LDO circuit design into challenge when the external off-chip capacitor which is used for stability compensation had to be removed (Raducan & Neag, 2015; Yun, Yun, & Kim, 2017).

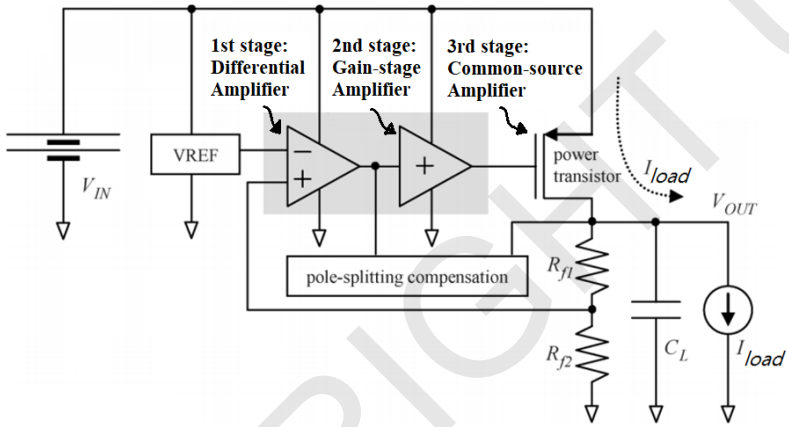

Figure 1.3: LDO design for SoC application

The LDO is viewed as a three-stage amplifier. The first stage amplifier is a differential amplifier. The second stage amplifier is a gain-stage amplifier. These two stages amplifier formed the error amplifier for the LDO. The third stage amplifier is the power PMOS transistor which is used to source high output load current. The large size of power PMOS contributes high parasitic capacitance at its gate terminal. Therefore the dominant pole for LDO in SoC application has shifted to the gate terminal of power PMOS transistor. To maintain a robust loop stability comes into challenge when the LDO needed to source a wide range of output load current from zero current to hundreds of milliampere (mA). The wide range load current has caused large variation of output impedance at LDO output node. The worst case scenario happen during zero load current where output impedance is too large and causing second pole shifted to lower frequency, hence compromise the loop stability of LDO system.

There are many reported LDO design to resolve the stability issue of SoC integrated LDO. There is a suggestion to use NMOS transistor instead of PMOS for the source follower in order to obtain low output impedance at the output of LDO (Day & Lie, 2011). This method sustain low impedance at output node over the wide range of load current and keep this pole at higher frequency. However the trade-off is that NMOS pass transistor has higher dropout voltage, thus achieving lower efficiency. There is also

another reported design imposing low-impedance at the output node of LDO (S. S. Chong & Chan, 2011). However excessive amount of current is needed in order to sustain the output in low impedance, hence resulting in higher quiescent current and worse efficiency.

Above issues have caused the low efficiency of SoC integrated LDO, especially during low load current. The efficiency equation is given in Equation (1.1) as

$$\eta = \frac{V_{out}I_{out}}{V_{in}(I_q+I_{out})} \tag{1.1}$$

, where I_q the quiescent current is and I_{out} is the output load current. From the equation, if the load current is very large comparing quiescent current, a very high efficiency can be achieved. In the other way, efficiency become worst if load current is low. By observing the total usage time of electronic devices in a day, it is known that most devices are under sleep-mode or stand-by mode most of the time. Therefore, improving efficiency at low output load current is deemed to be important in order to prolong the stand-by period of devices. Hence, reducing quiescent current during low output load current is essential.

Concluded from the above problem statements, the first issue is the conventional BGR with 1.12V voltage output is no longer viable to provide voltage reference for low power LDO. Second issue is the excessive amount of current is normally required to sustain the loop stability of LDO during low load current. These current can be reduced when load current gradually increases. The third issue is the difficulty to maintain the loop stability of LDO during very low output load current condition. Furthermore to reduce the total quiescent current of the LDO that contributed to low efficiency is another challenge to deal with, especially during low output load current condition.

1.4 Research objectives

The proposed research work is carried out with the purpose of realizing quiescent current reduction of self-compensated LDO. The research objectives of this research work are:

1) To design a low power bandgap reference circuit with sub-1V output stage to supply a stable reference voltage for the proposed LDO.
2) To design a quiescent current self-reduction circuit on the proposed LDO which is able to perform current reduction during low load current.
3) To design a self-compensation circuit for the proposed LDO, with the capability to self-repair the worsen loop stability during low load current.
4) To further reduce the total quiescent current of the proposed LDO during low load current using circuit design technique, in order to improve the efficiency of the LDO.

The circuit design of the proposed LDO is implemented using $0.13\mu m$ CMOS process technology with 1.20V voltage supply. The proposed LDO together with bandgap reference are both fabricated into silicon chip and measurement is further conducted.

1.5 Outline of the thesis

This thesis consists of six chapters. In Chapter 1, the introduction section discuss the current technology development trend and the current market demand for LDO, especially on the demand of SoC integrated LDO. The motivation of this research work has been validated. The problematic issues of LDO in SoC application is analyzed and described. And the list of research objectives for this work are being ruled out from here. Chapter 2 is the literature review chapter. Firstly, the performance parameters of LDO is being listed and explained in brief. Then the literature reviews on LDO is being discussed based on categories such as "low quiescent current LDO" review, "external capacitor-less LDO" review, and "LDO with enhancement topology" review. The trade-off on the performance parameters between these research papers are discussed. Chapter 3 discusses the design consideration on the circuit design of the proposed LDO that has to be taken into concern before any design work being carried out. The process technology constraint is discussed where the characteristic and limitation of transistors used in this work is being analyzed. Then the circuit design related constraint such as headroom and power transistor design are mentioned. The correlation between the LDO output load characteristic and its frequency response is being analyzed and discussed. Transient response is mentioned in the next section. In the following section, a circuit design methodology called inversion coefficient is introduced. Then the design trade-off that has to be made in this proposed LDO design is described. In Chapter 4, a sub-1V output stage bandgap reference (BGR) design is proposed. Firstly, the BGR design methodology is discussed. They are including the matching issue, V_{EB} of the PNP transistor, and issue pertaining BGR integration with LDO. Secondly, the principle of circuit operation is explained, then the circuit design of BGR is presented and described in subsection such as bandgap core circuit, start-up circuit, output stage circuit and op-amp circuit. Thirdly, the results and discussions are presented by subsection, including PVT impact on V_{REF}, and start-up circuit. An overall conclusion is presented at the end of this chapter. In Chapter 5, a self-compensation quiescent current reduction LDO is suggested. Firstly, the design methodology is discussed. Secondly the proposed LDO's circuit operation is described. They are including error amplifier and power PMOS, low impedance circuit, and sensing and control (SAC) circuit. Thirdly, analysis on the LDO loop stability is being discussed. The stability analysis comes with two different phenomenon which are high load current phenomenon and load current below 100μA phenomenon. Fourthly, the fabrication and measurement set-up are mentioned. The layout of the proposed LDO is shown in this section. Fifthly, the results and discussions of the proposed LDO is presented, including the measurement results. They are divided into three parts which are the results of stability and self-compensation, the results of quiescent current reduction and efficiency, and the results of DC voltage performance. An overall conclusion on the LDO design is made at the end of this chapter. A final conclusion is presented in Chapter 6. The contribution and the impact of this dissertation is presented, and the future research works are mentioned in this chapter.

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