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Reversible Palm Vein Authenticator Design With Quantum Dot Cellular Automata for Information Security in Nanocommunication Network

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ABSTRACT Palm vein pattern recognition is one of the most promising and rapidly developing fields of study in biometrics, which makes it an important solution for identity security in biometrics-based user identification systems. Quantum-dot Cellular Automata (QCA) is a developing field of nanotechnology which facilitates the creation of nano-scale logical circuits. Irreversible technology has faced some difficulties, such as higher heat energy dissipation. Reversible logic is therefore essential where heat dissipation is almost insignificant. This article proposes QCA design of a reversible circuit for palm vein authentication utilizing the Feynman gate. Fully reversible Feynman gate is designed. Using this newly designed Feynman gate the palm vein authenticator circuit is designed. The theoretical values and the results of the simulation correspond to the reliability of the planned circuit. Circuit complexity and circuit cost are explored. Validation of authenticated users by the proposed authenticator explores its design accuracy as per theoretical values. Energy dissipation of the proposed designs shows that it remains within Lauderer's limit (0.06meV). This proves that the circuits designed are fully reversible in nature and dissipates very less amount of energy. Comparison with recent QCA state of the art architectures explores its characteristics.

INDEX TERMS Nano-electronics, QCA, majority logic, security, Feynman gate.

I. INTRODUCTION

QCA [1]–[6] is a developing field among different developing nano-electronic innovations that give a progressive move towards the nano level. In the course of the most recent decades, the microelectronic manufacturers have been upgrading in terms of speed and size of electronic gadgets. These advancements are in relevance to Moore's Law for a protracted time, which predicts that the quantities of gadgets incorporated on a chip will increase by twofold at regular intervals of eighteen months [7], [8]. It is possible to accomplish it through consistent and fast upgrades in every part of the incorporated circuit manufacture. This allows manufacturers to reduce the size of chip whereas increment the chip measure, while keeping up adequate yields. This is designed by architects and circuit designers systematically to minimize the chips' magnitude and reduce the operative current.

The unremitting advancement in gadget creation on the milli-micron scale is not solely confined due to the process of its creation, in addition to this, elementary issues rise from scaling, like quantum-mechanical impacts and extreme power dissipation. The tunnelling current of the gates is increased with the degree of minimization to submicron level for MOS (metal– oxide– semiconductor) gadgets. It has been estimated from different investigations that reduction in the size of devices is drawing nearer to its physical cut-off points. The two unique conditions can be utilized to pass on a rationale variable in two legitimate rationale states, for example, electronic spin during any physical circumstance. In an alternative way, this logic can be represented by Quantum effects. QCA [9]–[14] is among the Quantum logic devices which follow this logic.

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Circuit depends on QCA have the advantage of high density, fast switching and low power utilization. Further, it has benefits of highly parallel processing. In recent years QCA [15]–[21] is utilized to accomplish high density, fast exchanging rate, and its ability to operate at room temperature. Different combinational circuit [22], [23] and sequential circuit representation based on QCA has been suggested in recent years but few investigation endeavours with its application in the field of communication. This article endeavours with the application field.

The palm vein validation [24]–[26] has an elevated state of confirmation accuracy because of the uniqueness and unpredictability of the vein outlines of the palm. The pattern of palm vein lies within the human body, thus it is impossible to falsify.

Additionally, the framework is contactless and sterile for use in public. It is more dominant than other biometric confirmation, in comparison to face detection, iris detection, and retina detection. Palm vein verification employs infrared rays to infiltrate through the user's hand whenever the user holds his hand above the sensor. This extracts the veins information of the user's hand. Dark lines of veins are returned which helps in authentication.

Using QCA a reversible Palm Vein Authenticator (PVA) circuit has been designed which is smaller in size and also robust in performance.

The article's effectiveness is delineated as:

- Reversible majority gate is used to achieve the fully reversible QCA circuit of the Feynman gate.
- A reversible Palm Vein authenticator using the Feynman gate is designed and implemented using QCA technology.
- The designed QCA Feynman gate is contrasted with previously built circuits.
- Authenticated user validation is also performed via the proposed authenticator.
- Verification of the design's accuracy is demonstrated by theoretical values.
- Circuit complexity and circuit cost is calculated for the proposed design.
- The proposed majority gates are compared with state of art majority gates.
- Energy dissipation is calculated using QCA Designer-E and it is lesser below Lauderer's limit.
- The proposed PVA architecture is contrasted with recent QCA architectures.

The article is segregated into ten sections. Background of QCA is explored in section II. Related works are shown in section III. Then section IV explores the theoretical background of the palm vein authenticator. The proposed work is explained in Section V. The architecture designs of the proposed work have been explored in Section VI. Simulation result analysis of Feynman gate and Palm Vein Authenticator is provided in Section VII. In Section VIII discussion is done on the circuit's complexity, cost calculation, comparison with prevailing constructs, validation, the quantum cost, the proposed majority gate contrasted with existing majority gate and the proposed design is also contrasted with existing designs. Section IX presents the future work. Section X entails the conclusion part.

II. QCA BACKGROUND

QCA cell is the fundamental computing unit of QCA. It is of square form with tetrad quantum wells. Electrons are present inside these two tetrad wells. They occupy the diametric positions inside the cell due to Coulombic repulsion. Tunnelling activity takes place inside the cell due to polarization. Thus, two configuration states in QCA cells are present. They reflect binary "0" and "1" denotes -1 and $+1$ polarization and are denoted by the letter P, respectively. A QCA cell is displayed in Fig.1.

QCA wire is composed of several cells aligned adjacent to one another, shown in Fig. 2(a). NOT gate is constructed in QCA by placing the cells in oblique orientation as depicted in Fig. 2(b).

Other logic gates designed from majority gates are OR gate and AND gate. A three input majority gate comprises five QCA cells. Majority gate expression is represented as M (a,b,c) = ab + bc + ac. OR gate is designed by setting one of the three inputs to polarization $+1$, whereas AND gate is designed by setting one of the three inputs to polarization -1. The designs are shown in Fig. 3. Both inverters and other two logic gates are used for implementation of other logic functions.

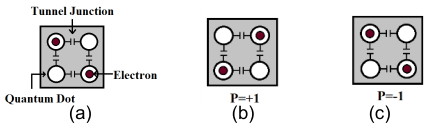

FIGURE 1. (a) QCA cell, (b) Binary 1(P= +1) (c) Binary 0 (P = −1).

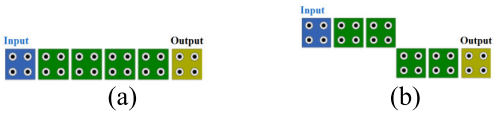

FIGURE 2. QCA (a) wire (b) NOT gate.

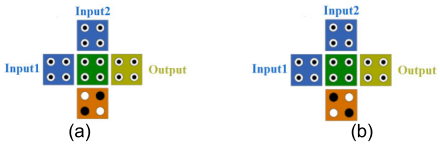

FIGURE 3. QCA (a) OR gate (b) AND gate.

III. RELATED WORK

In the past few years, works are done in the field of nano communication, image processing, and data security, utilizing QCA. The works explored in [27]–[31] are related to the field of nano-communication. In [27] a nano-sensor

processor has been produced. Different functionality can be performed by the processor. In this article, the procedure to process the data has been explained and how this preprocessed data is used to obtain a sigmoid function is explored. In [28] a serial nano-communication framework has been constructed which consists of serial-to-parallel and it's vice versa communication, parity checker, and Hamming code initiator. The reversible technique has been employed in the field of nano-communication in [29]. A QCA reversible router is publicized in this article. It employs less number of cells compared to other routers constructed beforehand. JK, SR, D, and T Flipflop's reversible architecture has been proposed in [30]. A reversible crossbar switch is exhibited in [31]. It shows the strategy of the activity of switches utilized throughout nano-communication. In correlation with the current traditional circuit, it's more cost-productive.

Data security during nano-communication is conferred in [32]–[34]. Security is provided during nano-communication by producing Ciphertext, realized using QCA in [32]. A serpent block cipher is designed in QCA to build the basic building block to obtain a block cipher. In [33] LSB bit steganography is explored using QCA. A secured text has been hidden within the LSB bit of an image and delivered to the sender. Information theory is used to enhance security. Reversible logic is used to reconstruct the LSB bit circuit for steganography to obtain a more dynamic version before the aforementioned circuitry in [34]. The complexity of the circuit has been calculated.

The arena of image processing doesn't remain immaculate by QCA, they are reported in [35]–[38]. A multichannel filter is designed in [35] utilizing QCA. The image threshold utilizing QCA has been accounted for in [36]. Median filtering is achieved in [37], applying QCA technology. In [37] usage of median filtering and effect of numerical procedures are seen over images, understood utilizing QCA based designs. One of the basic functionality of image processing is identified by the procedure convolution and correlation is performed in [38].

IV. THEORETICAL BACKGROUND

A. PALM VEIN AUTHENTICATION PROCESS

Palm vein authentication is the process of comparing the outlines of veins present in the palm of an individual with a sample present within the database. Vascular patterns on a palm vary from one person to another, as indicated by Fujitsu's research which is even indistinguishable between the twins. Since the vascular pattern exists inside the body, they can't be stolen by methods for photography, fingerprints or voice recording, consequently making this strategy for biometric confirmation more secure than others. Due to this threat, palm vein verification gives a progressively secure strategy for validation and thus presently creating enthusiasm as a biometric option in contrast to conventional current techniques for confirmation like PINs or passwords.

As indicated by BIOGUARD palm vein innovation works by recognizing the subcutaneous vein designs of hand. At the point when a client's hand is held over a scanner, infrared light maps the area of the veins. The red platelets present in the veins assimilate the beams and appear on the guide as dark lines, though the rest of the hand structure appears as white. This vein pattern is checked against a preregistered sample to verify the person. As veins lie within the body and have a lot of distinguishing features, it is not easier to detect which endeavors a higher level of security. Furthermore, the sensor of the palm vein gadget can perceive the vein pattern only if the hemoglobin is effectively streaming inside a person's veins.

B. DIFFERENT PRE-PROCESSING STEPS WITH A PARTICULAR PALM VEIN IMAGE

In Fig. 4 the different preprocessing steps are represented using a flowchart. Fig. 5 shows different steps performed on a sample palm vein image. The final image is a normalized binary image in which every pixel has a value of "0" or "1". These pixel values are either stored in the database and used later for testing, or fed into a palm vein authenticator system. The steps involved in conversion are:

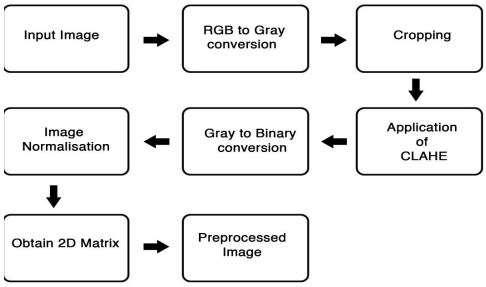

FIGURE 4. Different preprocessing steps of a palm vein image.

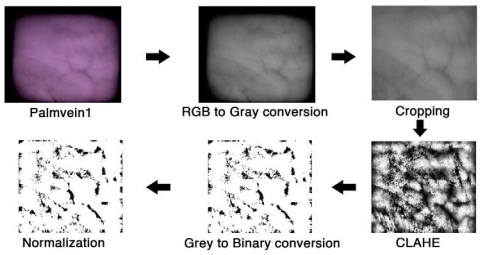

FIGURE 5. The actual output obtained after different preprocessing steps of a particular palm vein image.

- The RGB image is transformed to a Grayscale image.
- Then the image is cropped to acquire the required portion.
- Thereafter applying Contrast Limited Adaptive Histogram Equalization (CLAHE), the variance of the image is enhanced.
- In the next step, the image is converted from a grayscale to a binary form.
- Image Normalization is then applied to normalize the image.

- The image information is extracted in the form of a 2-D matrix which contains ''1'' and ''0'' only.
- Now the preprocessed data is ready either for providing input to the PVA or to be stored in the database.

A sample image ''Palmvein1.jpg'' is taken and the image undergoes the steps aforementioned to obtain the preprocessed image.

V. PROPOSED WORK

A. OVERVIEW OF THE PROPOSED SYSTEM

Initially, some palm vein images undergo preprocessing and the output binary data is stored within the database. A palm vein image is taken as input from the user. This image undergoes the various preprocessing steps. The preprocessing part is processed in MATLAB as shown with dotted lines in Fig. 6. The second input of the PVA is accepted from the already preprocessed data stored in the database. The binary data that is obtained from the image is fed into the QCA Palm Vein Authenticator (PVA) circuit as one of the inputs and another input comes from the database. The authentication part is shown in Fig. 3 comprises two sets of preprocessed images and QCA Palm Vein Authenticator (PVA). The PVA validates whether the user is authenticated or not. The step-by-step diagram of the proposed system is displayed in Fig.6.

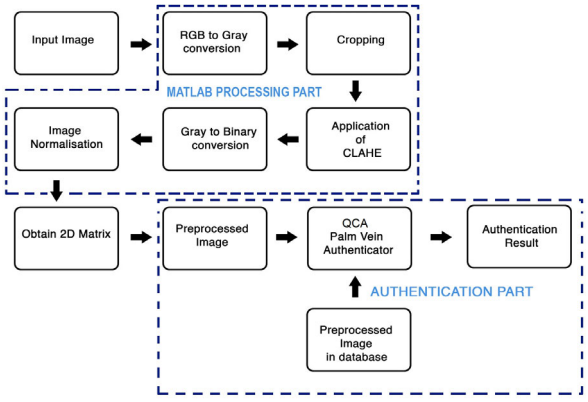

FIGURE 6. Overview of the proposed system with preprocessing part.

PVA is used to identify a user is a valid user or not. The main functionality of the PVA circuit is to compare two palm vein images and if both the palm vein images resemble then the user is genuine one otherwise not. If both the input bits are identical then the output is ''1'' otherwise if the input bits are diverse the output is ''0''. From this information, the truth table is generated where X and Y represent the inputs, and PVA_{out} represents the output. The truth table of PVA is exposed in Table 1. Karnaugh-map is drawn from Table 1 explored in Fig.7. When all of the output bits are ''1'' generated from the circuit then the user is a valid user otherwise invalid use.

The equation derived from the given K-map is

$$PVA_{out} = \overline{X} \cdot \overline{Y} + X \cdot Y \quad (1)$$

TABLE 1. The truth table for proposed palm vein authenticator.

X	Y	PVA_{out}
0	0	1
0	1	0
1	0	0
1	1	1

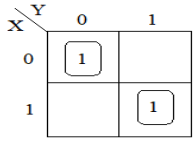

FIGURE 7. K-map for output of PVA circuit.

B. ALGORITHM FOR AUTHENTICATION OF PALM VEIN IMAGE OF A USER USING

The subsequent algorithm, Algorithm 1 describes the steps to perform an authentication test using the proposed palm vein authenticator circuit. An 8 X 8 matrix of values, i.e. 64 pixels per image (both user input and database image) are taken to simplify the process.

Algorithm 1

Input: Two 8×8 matrices of intensities of pixel data taken from preprocessed palm vein images. One is stored in the database; the other is taken from the user as input. This is converted into binary data and stored in two 64×64 pixels.
Output: Either '0' or '1'.
Initialization: Initialize P [64][64] = 0 (This matrix store the binary information of the input image)
Initialize M [64][64] = 0 (This matrix store the binary information of the image stored in the database)
Initialize T [64][64] = 0 (This matrix store sequence of output generated from PVA_{out})

Step 1: Read the binary values of a palm vein image from user input and in a matrix P [64][64] it is stored.
Step 2: Read the binary values of a palm vein image from the database and in a matrix M [64][64] it is stored..
Step 3: Match each and every value of P [64][64] with every corresponding value of M [64][64].
Step 4: For every comparison in Step 3,
If a match is found between the values of P and M, store '1' in the corresponding position in the T matrix, i.e.
Set T[i][j]: = 1;
Else store '0' in the corresponding position in T matrix, i.e.
Set T[i][j]: = 0.
Step 5: If all values of the T matrix are found to be 1, then the palm vein images are similar and the user is authenticated. Otherwise, the user is rejected.

VI. ARCHITECTURE FOR THE PROPOSED METHOD

A. QCA FEYNMAN GATE

Feynman gate is a 2×2 reversible gate, as depicted in the block diagram in Fig. 8. Two inputs INP1 and INP2 are

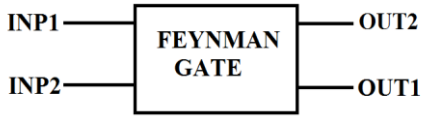

FIGURE 8. Block diagram of Feynman gate.

mapped along with two outputs OUT2 and OUT1. The relation between the inputs and the outputs are given by the expressions (2) and (3).

$$OUT1 = INP1 \oplus INP2 \tag{2}$$
$$OUT2 = INP1 \tag{3}$$

Formerly logically reversible QCA Feynman is designed in [39], [40] using standard majority gate as displayed in Fig. 3(a). A modified reversible majority gate is designed, in accordance with articles [41]–[43] is displayed in Fig. 9(a). Reversible OR and AND gates are designed from this majority gate and depicted in Fig. 9(b) and Fig.9(c) respectively. The majority gate has 3 inputs (A, B, C) and 3 outputs (GAR1, OUT, GAR2). GAR1 and GAR2 show the copy of inputs, A and B as output respectively. OUT shows the majority value of the input as output. The OR and AND gate consists of 3 inputs and 3 outputs. One input among these three inputs of the majority gate is set to P= +1 and P = −1 respectively. OUT of OR and AND gate functions as simple OR and AND gate respectively. These circuits function on Landauer's clocking as mentioned in [43].

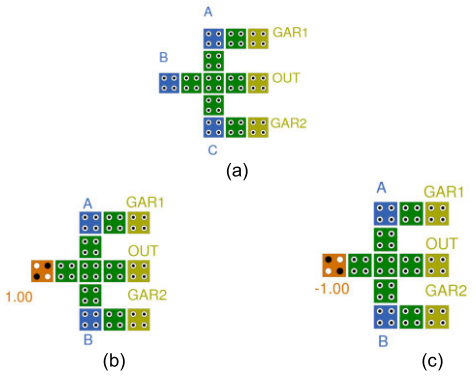

FIGURE 9. Reversible (a) Majority (b) OR (b) AND gate.

To design a fully reversible Feynman gate, the OR gate and AND gate designed in Fig.9(b) and Fig.9(c) are used. Since reversible basic gates are used to design the Feynman gate the block diagram of a fully reversible Feynman gate is different compared to Fig. 8 as revealed in Fig.10. Three additional inputs are fixed inputs having fixed inputs, FINP1(with P = −1), FINP2(P = −1) and FINP3(P = +1) respectively. Three garbage outputs GAR2, GAR3, and GAR4 are three. It should be noted that the number of inputs and outputs remains the same which follows the rule of reversibility of the circuit.

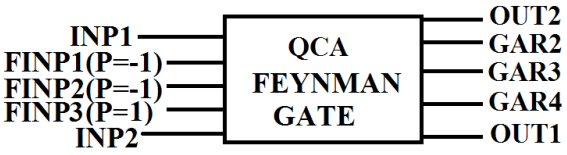

FIGURE 10. Block diagram of Feynman gate.

The expression for OUT2 and OUT1 is the same as eqn. (2) and eqn. (3) respectively. Three garbage values GAR2, GAR3, and GAR4 are added since fully reversible basic gates are used. New garbage values are provided in expressions (4), (5), and (6).

$$GAR2 = INP2 \tag{4}$$
$$GAR3 = INP1 \cdot \overline{INP2} \tag{5}$$
$$GAR4 = \overline{INP1} \cdot INP2 \tag{6}$$

The circuit diagram, QCA representation, and truth table of Feynman gate are revealed in Fig. 11 (a), (b), and Table 2 respectively. Reversible AND and OR gates are shown with dotted lines in Fig. 11(b). The hypothetical outputs for corresponding inputs of Feynman gate are shown in the Truth Table represented in Table 2.

TABLE 2. Truth Table of Feynman gate.

Input		Output				
INP1	INP2	OUT1	OUT2	GAR2	GAR3	GAR4
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0

B. REVERSIBLE PALM VEIN AUTHENTICATOR USING QCA

For designing fully reversible Palm Vein Authenticator (PVA), an additional NOT gate is added to the Feynman Gate shown in Fig.10. This adds the Feynman gate's unique features to realize the proposed reversible PVA is displayed in Fig. 12.

It is noted from Fig.12 and Fig.13 the PVA circuit design is created from the fully reversible Feynman gate as depicted in Fig.10 and Fig.11 respectively. To function the Feynman gate as fully reversible each of the modules are made reversible. The reversible majority gate included in this design is similar to the articles [41]–[43]. The majority gate consists of three inputs and three outputs. Copies of inputs are obtained as outputs on two of the outputs and the middle one gives the resultant output. It eliminates the fanout problem. The Feynman gate design has two main inputs INP1 and INP2 and three fixed inputs with polarization FINP1(with P = −1), FINP2(P = −1) and FINP3(P = +1) respectively. It consists of two main outputs OUT1 and OUT2 respectively and three garbage values GAR2, GAR3 and GAR4. All of these garbage values actually denote the copy of their input values. GAR2 denotes the value same as INP2. GAR3 denotes

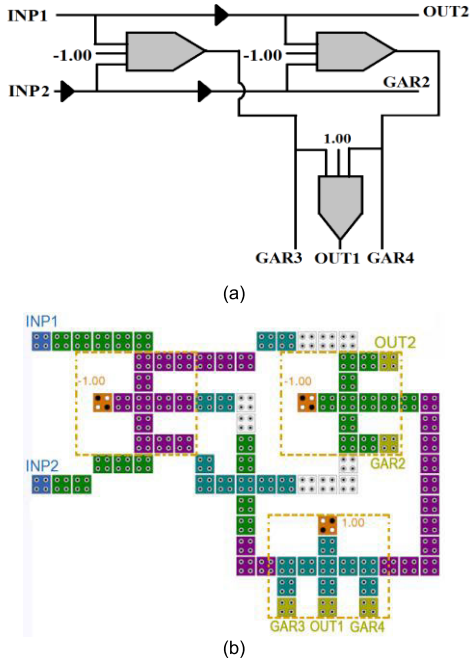

FIGURE 11. Proposed Feynman Gate (a) Circuit diagram (b) QCA representation.

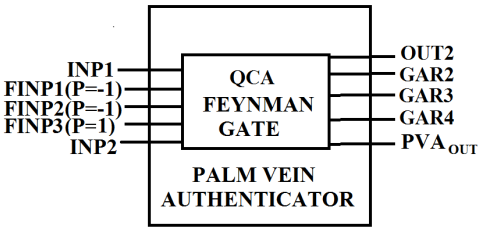

FIGURE 12. Block diagram of proposed reversible Palm Vein Authenticator circuit.

output value obtained from the first AND gate, similarly GAR4 denotes the output obtained from the second AND gate.

Feynman gate is a reversible gate which functions as an XOR gate. The designed PVA acts as an XNOR gate. The comparison is done between two bits to check if either bit is similar, then the result is true otherwise false. When a NOT-gate is positioned after the Feynman gate's output, OUT1 the required output will be obtained at PVA_{out} as represented in expression (7).

$$PVA_{out} = INP1 \cdot INP2 + \overline{INP1} \cdot \overline{INP2} \tag{7}$$

The other expressions for garbage are similar to expressions (3), (4), (5), and (6). Expression (7) shows that PVA_{out} actually functions as an XNOR gate. The XNOR gate output remains true only when both of the inputs are similar.

The fully reversible PVA receives the palm vein information from an user in the form of binary values obtained after preprocessing of the palm vein image in MATLAB and validate the information with the database of preprocessed images previously exists using the proposed QCA Palm Vein Authenticator. If the information matches, the input palm vein image is confirmed as a valid palm vein image, and the user is authenticated, otherwise it is treated as an invalid palm vein image and the user is not authenticated.

The block diagram of PVA is displayed in Fig. 9. Its circuit diagram, QCA layout, and corresponding truth table are explored in Fig. 13(a), 13(b), and Table 3 respectively. Landauer's clock is applied to the PVA circuit as referred to in [43] to reduce the power dissipation. The process of authentication of user palm vein image is carried forward using the proposed reversible PVA circuit as described in Algorithm 1.

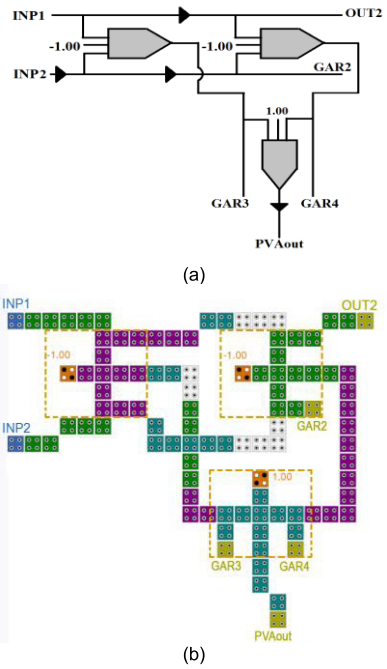

FIGURE 13. Proposed Palm Vein Authenticator's (a) Circuit diagram (b) QCA layout.

TABLE 3. Truth Table of palm vein authenticator.

Input		Output				
INP1	INP2	PVA_{out}	OUT2	GAR2	GAR3	GAR4
0	0	1	1	0	0	0
0	1	0	1	1	0	1
1	0	0	0	0	1	0
1	1	1	0	1	0	0

VII. RESULTS

A. SIMULATION RESULTS OF FEYNMAN GATE

The simulation result of the Feynman gate circuit using the QCADesigner-E tool [44], [45] is shown in Fig 14. From the third clock pulse, the output OUT1 is observed. The sequence of input in the first input signal INP1 is "00110011" and in the second input signal INP2 is "01010101". OUT1 is one

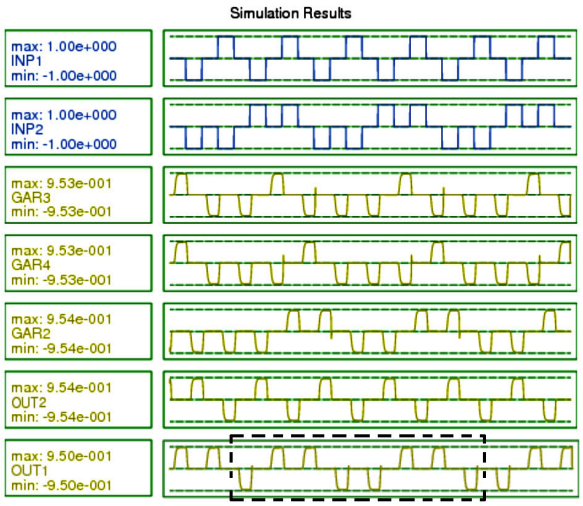

FIGURE 14. Simulation results of Feynman gate.

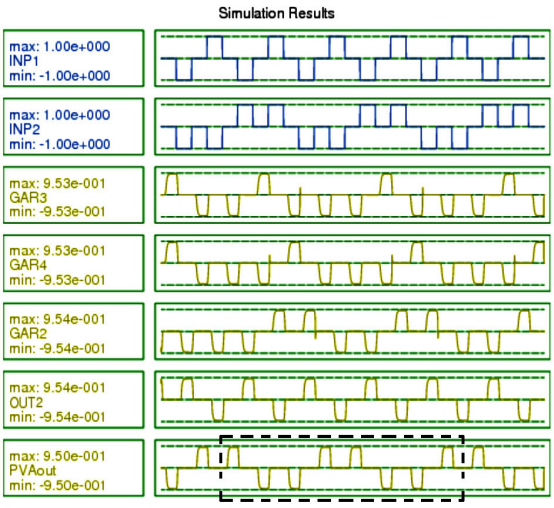

FIGURE 15. Simulation results of palm vein authenticator.

of the output signals. The other outputs are OUT2, GAR2, GAR3, and GAR4. The outputs of OUT1, OUT2, GAR2, GAR3, and GAR4 correspond to equation (2), (3), (4), (5), and (6) respectively as portrayed in Fig. 14. The output OUT1 is shown with dotted lines in Fig.14.

B. SIMULATION RESULTS OF PROPOSED PALM VEIN AUTHENTICATOR

The simulation result of the proposed Palm Vein Authenticator circuit is displayed in Fig 15. From the third clock pulse, the output PVA_{out} is observed. The sequence of input in the first input signal INP1 is ''01010101'' and in the second input signal, INP2 is ''00110011''. OUT2, GAR2, GAR3, GAR4, and PVA_{out} are the output signals. The outputs of OUT2, GAR2, GAR3, and GAR4 correspond to equation (2), (4), (5) and (6) and PVA_{out} respectively corresponds to the equation (7) as portrayed in Fig. 15. The output PVA_{out} is shown with dotted lines in Fig.15.

VIII. DISCUSSIONS

A. PARAMETERS USED IN QCA DESIGNER

The parameters set used in QCA Designer-E [45] to obtain the proposed circuit's simulation results as well as energy dissipation, is depicted in Fig. 16. These are the basic parameters for the QCA Designer-E tool to simulate the circuit. Both the height and the thickness of one QCA cell are 18nm. The spaces between each QCA cell are 2nm. The area of the QCA design is calculated including the space between the cells.

Two sets of parameters are explained in [45] and observed in Fig.17, are in accordance with Fig.16 used during simulation. Fig.17(a) represents technology parameters and Fig. 17(b) represents the simulation parameters.

B. CIRCUIT COMPLEXITY

Table 4 explores the complexity of the proposed circuits. The number of majority voter gates (MVs), number of QCA cells

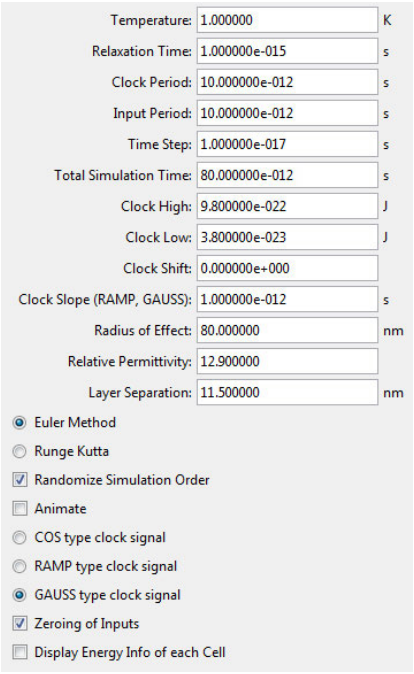

FIGURE 16. Set of parameters used during simulation in QCA Designer-E.

used i.e. the cell count, total area, cell area, percentage of area utilized, and the latency are stated in the table.

C. COMPARISON WITH EXISTING FEYNMAN GATES

The proposed Feynman gate is compared with some existing designs reported in [46]–[50] Table 5, in terms of the number of cells, areas employed, delay, several layers, and reversible approach used.

It is noted from Table 5 that the proposed Feynman gate is higher in terms of the amount of cells, area employed, and delay than other existing designs [46]–[50]. It is observed from Table 5 that the proposed design is functioning as a fully reversible gate. Each of the modules of the design is

TABLE 4. Circuit complexity of the proposed circuits.

Proposed QCA circuit	Number of MVs	#Cell	Entire Area (μm^2)	Area acquired by the Cells (μm^2)	Area Utilized	Latency (clock cycle)
Feynman Gate	3 MVs and 2 inverters	90	0.112	0.036	32.14	1.75
Palm Vein Authenticator	3 MVs and 3 inverters	99	0.152	0.0396	26.05	1.75

TABLE 5. Comparison with existing Feynman gates.

Feynman Gate	No. of Cells	Area	Latency	Layers used	Reversibility
Proposed Feynman Gate	90	0.112	1.75	Single-layer	Fully Reversible
[46]	69	0.070	1.00	Multi-layer	Logical
[47]	78	0.090	1.00	Single layer	Logical
[48]	89	0.102	1.00	Single layer	Logical
[49]	56	0.066	0.75	Single layer	Logical
[50]	27	0.0196	0.75	Single layer	Logical

obtained by using reversible majority gates. Landaeur's clock is employed to ensure it is fully reversible.

D. USER VALIDATION WITH PROPOSED CIRCUIT

Figure 17 depicts the method of authentication. As shown in the figure, the first eight-bit of the input image is provided to the PVA, similarly, the first eight bits of the image present in the database are recovered, and thereafter both the bits are matched in a bitwise manner. If bit values of both images are same such as ("0" & "0") or ("1" & "1") then the output will be "1", similarly if the bit values are different such as ("0" and "1") or ("1" and "0") then the outputs are "0". As shown in Fig. 17(a) all of the outputs obtained from the eight bits are "1" and similarly for the total image the output is "1" then the user is valid. In Fig. 17(b) all of the outputs for the first eight bits are not "1" and therefore correspondingly for the total image the outputs are a mixture of "1" and "0", then the user is not valid. These two cases are studied and represented in **Case Study 1** and **Case Study 2** respectively

Case Study1:

The first input signal, INP1 is "00110011" and the second input signal, INP2 is "00110011", which is stored in the database as depicted in Fig. 19. The output observed from the third clock pulse. From Table 3 it is observed that when the two inputs are the same, as in either both inputs are 'LOW' or both inputs are 'HIGH' the output PVA_{out} is 'HIGH'. The output PVA_{out} becomes 'LOW' when one input is 'HIGH' and the other is 'LOW'. From the simulation result obtained in Fig. 19 it is observed that from the output, PVA_{out} is an entire sequence of 1's, which proves that both the images are matched and the user is valid.

Parameter	Description	Standard Value
QD size	Size of a quantum dot	5 nm
Cell area	Dimensions of each cell	18 nm x 18 nm
Cell distance	Distance between two cells	20 nm
Layer distance	Distance between QCA layers in case of multilayer crossing	11.5 nm
τ	Relaxation time	1E-15 s
γ_H	Max. saturation energy of clock signal	9.8E-22 J
γ_L	Min. saturation energy of clock signal	3.8E-23 J
ϵ_r	Relative permittivity of material for QCA system	12.9[I]
Temp	Operating temperature	1 K
r_{effect}	Maximum distance between cells whose interaction is considered	80 nm[II]

[I]Relative permittivity of GaAs and AlGaAs.
[II]Interaction effects between two cells decays inversely with the fifth power of its distance.

(a)

Parameter	Description	Standard Value
T_γ	Period of the clock signal	10E-12 s
γ_{slope}	Rise and fall time of the clock signal slopes	1E-10 s
γ_{shape}	Shape of clock signal slopes [RAMP/GAUSSIAN]	GAUSSIAN
T_{in}	Period of the input signals	10E-12 s
T_{sim}	Total simulation time	80E-12 s
T_{step}	Time interval of each iteration step	1E-17 s

(b)

FIGURE 17. Set of parameters used in QCADesigner-E [44] (a) Technology parameters (b) Simulation parameters.

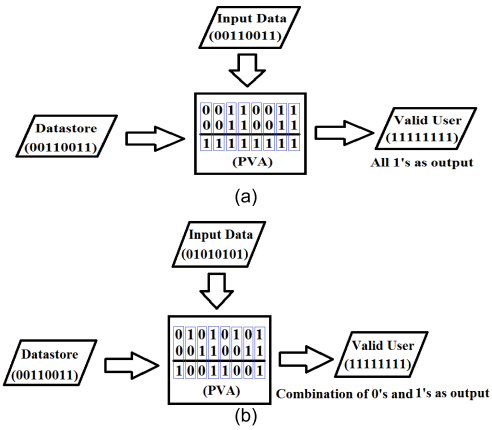

FIGURE 18. Validation Process (a) valid user (b) invalid user.

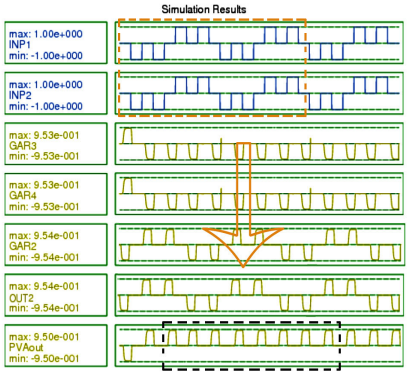

FIGURE 19. Simulation results of PVA for valid-user.

Case Study2:

The first input signal, INP1 is "01010101" and the second input signal, INP2 is "00110011". From the third clock pulse, the output is observed. As aforementioned, the

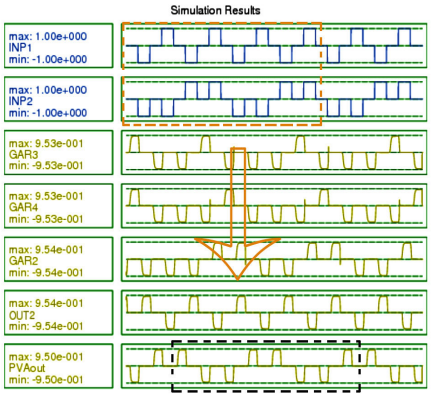

FIGURE 20. Simulation results of PVA for invalid users.

TABLE 6. Truth Table of palm vein authenticator.

Circuit Proposed	$Circuit_{cost}$ Function
A new Feynman Gate	39.8125
Palm Vein Authenticator(PVA)	42.875

simulation result obtained in Fig. 20 is in correspondence with Table 3. It is observed that from the output, PVA_{out} entire output sequence is not 1's which proves that both the images are not matched and the user is invalid.

E. CIRCUIT COST ESTIMATION OF THE PROPOSED CIRCUITS

The circuit cost of a QCA circuit can be calculated using QCA cost function as shown in Eqn. (8) [51], [52].It is composed of four parameters. "M" represents the quantity of majority gates used, "I" specifies the quantity of inverters used, "C" denotes the quantity of crossovers, and "T" denotes delay or latency present in the QCA circuit generated. The "C" term has some more description. It is one of the fundamental features depending on the number of wire crossovers. Two types of the crossover are present in the QCA circuit; they are coplanar crossover and multilayer crossover respectively. In the coplanar crossover, as its name suggests all the cells remain in a similar plane, different layers are created using different clock zones. Multilayer crossovers are composed of several layers. The assembly of a multilayer circuit in contrast to the coplanar circuit is considerably complex. The term "C" thus consists of two terms, C_{cp} and C_{ml}, where C_{cp} denotes the coplanar crossovers and C_{ml} denotes the multilayer crossover respectively. A relation persists between these two terms i.e. $C_{ml} = m \times C_{cp}$, m is considered to be equivalent to 3. "C" for equation (8) is calculated by equation (9). "k", "l", and "p" are powers of "M", "C" and "T" correspondingly. Each of the exponents mentioned is assigned with a value of 2 for calculation of circuit cost.

$$QCA_{cost} = \left(M^k + I + C^l\right) \times T^p, 1 \leq k, l, p \quad (8)$$

$$C = C_{cp} + C_{ml} = C_{cp} + m \times C_{cp} \quad (9)$$

TABLE 7. Comparison with existing Majority gates.

Majority Gate	#Cell	Area	Latency	No. of O/P	No. of Garbage O/P	Reversibility
Proposed 3-input Majority Gate (Fig. 9a)	13	0.01	0.25	3	2	Yes
Standard 3-input majority gate[36]	5	0.0036	0.25	1	0	No
Five input majority gate[53]	16	0.015	0.75	1	0	No
Seven input majority gate[54]	23	0.014	0.25	1	0	No

TABLE 8. Comparison with existing works.

QCA Architecture	Logical modules	#Cell	Area (μm^2)	latency	Reversible
Proposed PVA	3 MVs 3 IVs	99	0.152	1.75	Fully
Image masking [55]	48 MVs 32 IVs	712	0.86	2.0	No
Cryptographic architecture [56]	39 MVs 14 IVs	581	1.14	5.5	No
image Steganographic architecture [18]	24 MVs, 12 IVs	744	0.889	2.0	No
Cryptographic element [57]	Not mentioned	115	0.13	1.5	No
Cryptographic hardware [58]	Not mentioned	3485	25.80	20.75	No
Cryptographic architecture [59]	Not mentioned	4414	5.34	23.0	No
Image Steganography [34]	6 MVs, 4 IVs	483	0.335	2.5	Logical
User Password Authentication [39]	6 MVs, 4 IVs	84	0.091	0.75	Logical
Image Negative [60]	24 MVs, 19 IVs	Not mentioned	Not mentioned	Not mentioned	No

The reversible Feynman gate as presented in Fig. 8(b) Circuit cost calculated through equation (1) and (2) is depicted underneath. Quantity of M present here is 3, I is 3, and the crossovers, C_{cp} is 1 and C_{ml} is 0, and the latency is T = 1.75. The value of C is calculated from equation (9) as

$$C = 1 + 0(m = 3, \text{since no crossovers are present}) = 1$$

Substituting all the values in eqn. (8), the circuit cost will be

$$\begin{aligned} QCA_{cost} &= (3^2 + 3 + 1^2) \times 1.75^2 \\ &= (9 + 3 + 1) \times 3.0625 \\ &= 39.8125 \end{aligned}$$

TABLE 9. Power dissipation.

Circuits	For different Input Signal Combinations amount of Power Dissipation [meV]							
	000	001	010	011	100	101	110	111
Inverter (Fig.2(b))	0.001	0.001						
Reversible Majority gate (Fig.9(a))	0.003	0.003	0.003	0.003	0.003	0.003	0.003	0.003
Reversible OR (Fig.9(b))	0.002	0.003	0.002	0.002				
Reversible AND (Fig.9(c))	0.002	0.002	0.003	0.002				
PVA Circuit Designed (Fig. 13(a))	0.010	0.011	0.011	0.010				

Similarly the reversible Palm Vein Authenticator as presented in Fig. 10(b) circuit cost is calculated via equation (8) and (9) are depicted beneath. Quantity of M present here is 3, I is 4, and the crossovers C_{cp} is 1, and C_{ml} is 0, and the latency is T = 1.75. The value of C is calculated from Eqn. (9) as

$$C = 1 + 0 = 1$$

Substituting all the values in Eqn. (8), the cost will be

$$\begin{aligned} QCA_{cost} &= (3^2 + 4 + 1^2) \times 0.75^2 \\ &= (9 + 4 + 1) \times 3.0625 \\ &= 42.875 \end{aligned}$$

Table 6 demonstrates the QCA_{cost} for circuits in Fig. 8(b) and Fig. 10(b) respectively.

F. COMPARISON OF DESIGNED MAJORITY GATES WITH OTHER MAJORITY GATES

Four types of majority gates present in QCA technology till date [36], [53], [54]. In Table 7 these majority gates are compared in terms of quantity of cells, latency, area, number of inputs, number of garbage outputs and reversibility.

It is noted from Table 7 that the number of cells, and no. of outputs in case of the proposed 3-input reversible Majority Gate exceeded in quantity of cells and number of garbage outputs but it is reversible in nature.

G. COMPARISON OF DESIGNED PVA CIRCUIT WITH EXISTING QCA ARCHITECTURES

Some of the existing QCA architectures [18], [34], [39], [55]–[60] are compared with the propose PVA architecture in Table 8.

It is observed from Table 8 that Image Steganography and User Password Authentication reported in [34] and [39] are logically reversible whereas the proposed PVA is fully reversible in nature.

H. POWER DISSIPATION CALCULATION OF THE PROPOSED DESIGNS

The research provided in [41] shows that QCA NOT gate, reversible majority gate, reversible AND gate and reversible OR gate are reversible in nature. It is explored in [41] the power dissipation of these fundamental reversible gates is below (kBTln2) energy limit. The energy dissipation values for different input combinations (000-111) of these gates are explored in Table 9 with respect to the parameters depicted in Fig. 17. The energy dissipation value for the proposed reversible PVA circuit is calculated using QCADesigner-E and explored in Table 9. The value of energy dissipation of the PVA circuit is observed, which is below Landauer's limit (0.06meV).

IX. FUTURE SCOPE

In future a new RAM architecture will be designed in QCA. It will store the data obtained from MATLAB. Then via RAM the image data can be sent to the Palm Vein Authenticator Circuit designed in this article. Same mechanism will be followed for the data stored in the database using another RAM.

X. CONCLUSION

A novel reversible QCA-based Palm Vein Authenticator (PVA) is reported in this article. The proposed PVA is advantageous in escalating the security of data accomplished by the validation of a legitimate client. QCA utilized less power and denser nano-circuit for the proposed design. The truth table affirms the results clarifying the suitability of the circuit. The utilization of QCA upgrades the PVA circuit in two different ways. Validation of authenticated users by the proposed authenticator shows its design accuracy as per theoretical values. Circuit complexity and circuit cost have been calculated to explore its implementation cost. Energy dissipation is calculated to prove that the proposed design dissipates energy within Lauderer's limit. Comparison with recent QCA state of the art architectures explores its characteristics.

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