Reliability analysis of multibit error correcting coding and comparison to hamming product code for on-chip interconnect

ABSTRACT

Error control schemes became a necessity in network-on-chip (NoC) to improve reliability as the on-chip interconnect errors increase with the continuous shrinking of geometry. Accordingly, many researchers are trying to present multi-bit error correction coding schemes that perform a high error correction capability with the simplest design possible to minimize area and power consumption. A recent work, Multi-bit Error Correcting Coding with Reduced Link Bandwidth (MECCRLB), showed a huge reduction in area and power consumption compared to a well-known scheme, namely, Hamming product code (HPC) with Type-II HARQ. Moreover, the authors showed that the proposed scheme can correct 11 random errors which is considered a high number of errors to be corrected by any scheme used in NoC. The high correction capability with moderate number of check bits along with the reduction in power and area requires further investigation in the accuracy of the reliability model. In this paper, reliability analysis is performed by modeling the residual error probability Presidual which represents the probability of decoder error or failure. New model to estimate Presidual of MECCRLB is derived, validated against simulation, and compared to HPC to assess the capability of MECCRLB. The results show that HPC outperforms MECCRLB from reliability perspective. The former corrects all single and double errors, and fails in 5.18% cases of the triple errors, whereas the latter is found to correct all single errors but fails in 32.5% of double errors and 38.97% of triple errors.

Keyword: Error correctioncodes; Multi bit error; On chip interconnect; Residual error rate