Optimized low voltage low power dynamic comparator robust to process, voltage and temperature variation

ABSTRACT

Power consumption and speed are the main criteria in designing comparator for analog-to-digital converter (ADC). This paper presents an optimized low voltage low power dynamic comparator which is robust to process, voltage and temperature (PVT) variations with adequate speed. The comparator circuit was designed using 0.18µm CMOS technology with low voltage supply of 0.8V. The method used to verify the robustness of the comparator circuit across 45 PVT is presented. The circuit is simulated with 10% voltage supply variation, five process corners and temperature variation from 0°C to 100°C. The simulation result show that the proposed comparator circuit achieved significant reduction of power consumption and delay during worst case condition compared to dynamic comparator proposed from previous researchers.

Keyword: Dynamic comparator; Double-tail dynamic comparator; Low power comparator; ADC; SAR; ADC