OPTIMIZATION OF FAST FOURIER TRANSFORM BASED ON TWIDDLE FACTOR USING GENETIC ALGORITHM ON RASPBERRY PI

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By

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Chairman : Nasri Sulaiman, PhD
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The research work revolves around the 16-point Radix-4 Single Path Delay Feedback (R4SDF) for optimizing the pipelined Fast Fourier Transform (FFT) processor, which can be done by using both Single Objective Genetic Algorithm and Multi-Objective Genetic Algorithm , Nowadays in many areas of engineering and science are widely using FFT processors in most of their applications, thus, the modern science requires continuously new optimizations which includes the FFT processor to have a lower power consumption and a smaller size. However, both Signal to Noise Ratio (SNR) and Switching Activity (SA) values depend on the word length of the FFT processor, the bigger the word length of the FFT processor will result in a higher value for the SNR and the SA, Thus, this research aims to reduce the power consumption of the FFT processor by lowering the word length of Twiddle Factor for the FFT by using both Single Objective Genetic Algorithm (SOGA) and Multi-Objective Genetic Algorithm (MOGA) to find the optimum results for SNR and SA values while lowering the Word Length. Over the years the Genetic Algorithms (GA) proved to be one of the best methods for optimization. The proposed work will start by tasking the SOGA with modifying the SNR fitness function to secure the SNR value (which determines the accuracy factor) for the research to check if the research can obtain SNR value more than 63dB while lowering the word length of the Twiddle Factor, next is to reduce power consumption by tasking MOGA with finding the SA values below 192 (SA values determine the power consumption) while maintaining the SNR values above 63dB, then is to evaluate both of SOGA and MOGA results to compare with the results of the default parameters of the most relevant research. In this research the GA is for reducing the word length by optimizing its coefficients. The required amount of value for the SNR is to be more than 63 dB and for SA is to be lower than 192. The proposed work was done successfully in optimizing the FFT by using SOGA to lower the word length until 12 bits and obtaining a SNR value of 66.452dB which resulted in an improvement of 5.47% for SNR, also, the optimization for the FFT was done successfully by using MOGA to lower the word length until 12 bits and obtaining a SNR value of 65.65dB which resulted in an improvement of 5.47% for SNR and a SA value of 134 which resulted in reduction to SA by 30.2%.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memnuhi kerperuan untuk ijazah Sarjana Sains

OPTIMISASI TRANSFORMASI FOURIER FASTIER BERDASARKAN FAKTOR DUA DENGAN MENGGUNAKAN ALGORITM GENETIC PADA RASPBERRY PI

Oleh

FIRAS FAISAL GHAZI

November 2019

Pengerusi : Nasri Sulaiman, PhD
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Kerja-kerja penyelidikan berkisar sekitar *Radix-4 Single Path Delay Feedback* (R4SDF) untuk mengoptimumkan prosesor jelmaan Fourier pantas(FFT) pipelined, yang boleh dilakukan dengan menggunakan Algoritma Genetik Algoritma Genetik dan Multi-Objektif Algoritma Genetik, Kini dalam banyak bidang kejuruteraan dan sains secara meluas menggunakan pemproses FFT dalam kebanyakan aplikasi mereka, maka sains moden memerlukan pengoptimuman yang berterusan baru yang termasuk pemproses FFT untuk mendapatkan penggunaan kuasa yang lebih rendah dan saiz yang lebih kecil. Walau bagaimanapun, kedua-dua nilai Isyarat Rintangan (SNR) dan Nilai Tukar (SA) bergantung pada panjang perkataan pemproses FFT, semakin besar panjang perkataan pemproses FFT akan menghasilkan nilai yang lebih tinggi untuk SNR dan SA, Jadi , penyelidikan ini bertujuan untuk mengurangkan penggunaan kuasa pemproses FFT dengan menurunkan panjang perkataan Faktor Twiddle untuk FFT dengan menggunakan Algoritma Genetik Objektif Single (SOGA) dan Algoritma Genetik Multi Objektif (MOGA) untuk mencari keputusan optimum untuk SNR dan nilai SA semasa menurunkan Panjang Word. Selama bertahun-tahun Algoritma Genetik (GA) terbukti menjadi salah satu kaedah terbaik untuk mengoptimumkan. Kerja-kerja yang dicadangkan akan bermula dengan menugaskan SOGA dengan mengubah fungsi kecergasan SNR untuk menjamin nilai SNR (yang menentukan faktor ketepatan) untuk penyelidikan untuk memeriksa sama ada penyelidikan dapat memperoleh nilai SNR lebih daripada 63dB sambil menurunkan panjang perkataan Twiddle Faktor seterusnya adalah untuk mengurangkan penggunaan kuasa dengan menugaskan MOGA dengan mencari nilai SA di bawah 192 (nilai SA menentukan penggunaan kuasa) sambil mengekalkan nilai SNR di atas 63dB, maka kita menilai kedua-dua hasil SOGA dan MOGA dibandingkan dengan hasil parameter piawai penyelidikan yang paling relevan. Dalam kajian ini GA adalah untuk mengurangkan panjang perkataan dengan mengoptimumkan pekali-pekalinya. Jumlah nilai yang diperlukan untuk SNR adalah lebih daripada 63 dB dan untuk SA adalah lebih rendah daripada 192. Kerja yang dicadangkan telah berjaya dilakukan dengan mengoptimumkan FFT dengan menggunakan SOGA untuk menurunkan panjang perkataan hingga 12 bit dan memperoleh SNR nilai 66.452dB yang menghasilkan peningkatan 5.47% untuk SNR, juga, pengoptimuman untuk FFT berjaya dilakukan dengan menggunakan MOGA untuk menurunkan panjang perkataan hingga 12 bit dan memperoleh nilai SNR 65.65dB yang menghasilkan peningkatan 5.47% untuk SNR dan nilai SA 134 yang mengakibatkan pengurangan kepada SA sebanyak 30.2%.

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I certify that a Thesis Examination Committee has met on **Nov 2019** to conduct the final examination of **Firas Faisal Ghazi** on his thesis entitled Optimization of **Fast Fourier Transform based on Twiddle Factor using Genetic Algorithm on Raspberry Pi** in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master's degree

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVATIONS

BF	Butterfly Unit
DC	Delay Commutator
DF	Delay Feedback
DFT	Discrete Fourier Transform
DIF	Decimation In Frequency
DIT	Decimation In Time
DSP	Digital Signal Processing
FFT	Fast Fourier Transform
FIFO	First In First Out
GA	Genetic Algorithm
LSB	Less Significant Bit
MDC	Multiple Path Delay Commutator
MOGA	Multi-Objectives Genetic Algorithm
MSB	Most Significant Bit
R4SDF	Radix 4 Single Path Delay Feedback
SA	Switching Activities
SDC	Single Path Delay Commutator
SDF	Single Path Delay Feedback
SFG	Signal Flow Graph
SISO	Serial In Serial Out
SNR	Signal to Noise Ratio
SOGA	Single Objective Genetic Algorithm
TF	Twiddle Factor

CHAPTER 1

INTRODUCTION

1.1 Background

In Digital Signal Processing (DSP) the Fast Fourier Transform (FFT) is considered as the algorithm that transforms the signal from time domain to frequency domain which can be used in many applications in DSP such as image processing, telecommunication systems, sonar, radar, control systems, sensor array, and biomedical engineering [1]. Power consumption is one of the most critical problems in FFT processors. Therefore, the optimization of FFT for the reduction of power consumption has been done by other researchers using different methods such as proposing architecture or an algorithm, and according to previous researchers, there are two techniques that helps to reduce the power consumption, one of them is to design FFT architecture, the other one is to create an algorithm, the difference between these two techniques is that the design of architecture cannot be modified to get better results, while an algorithm can dynamically be changed and tasked to make a reconfigurable Twiddle Factor in order to get the best results, an example of an optimization by algorithm is to use the Genetic Algorithm which was proved by other researchers to be an effective method to optimize the Fast Fourier Transform, more details on the researchers use of GA will be discussed in chapter 2.

1.2 Genetic Algorithm

A Genetic Algorithm is a type of an evolutionary algorithm which can result with high quality of solutions to most complicated problems in a small amount of time. GA can be tasked as a Single Objective Genetic Algorithm (SOGA) or Multi-Objective Genetic Algorithm (MOGA) to do certain tasks to optimize the FFT [1]. (SOGA, MOGA and other FFT optimization methods) will be discussed in details in chapter 2.

1.3 Problem Statement

The FFT processor is the most critical block in digital communication systems (DSP) such as MC-CDMA receiver. Power consumption has been a major concern in the digital communication systems. The power consumption depends on the Word Length of the Twiddle Factor for the FFT processor, obtaining the Twiddle Factor will allow the SNR and SA to be calculated through SNR and SA equations in chapter 3 [2]. One way to reduce the power consumption in the FFT processor is to reduce the Word Length for the Twiddle Factor, to lower the Word Length, it must meet the target objectives for both of Signal to Noise Ratio (SNR) which is considered as the accuracy factor and Switching Activity (SA) which is considered as the power consumption factor [3], these factors will be discussed more in details in chapter 2. Most of the researchers who optimized the FFT processor used Genetic Algorithm, the Genetic Algorithm (GA) can be tasked to find the best solutions for the most complex problems, it can be tasked as a Single-Objective Genetic Algorithm (SOGA) or a Multi-Objective Genetic Algorithm (MOGA) [4] both of these approaches will be discussed in chapter 4 and chapter 5. The results of the proposed will be compared with the results of [1] who managed to get to 3.79% of SNR improvement for 13 bits of word length as the lowest bits of the word length value for SOGA, and also managed to get 5.35% of SNR improvement and 19.79 of SA reduction for the MOGA. The proposed work will start by tasking the SOGA with securing the SNR fitness function to secure the SNR value (which determines the accuracy factor) for the research to check if the research can obtain SNR value more than 63dB while lowering the word length of the Twiddle Factor, next is to reduce power consumption by tasking MOGA with

finding the SA values below 192 (SA values determine the power consumption) while maintaining the SNR values above 63dB, then is to evaluate both of SOGA and MOGA results to compare with the results of the default parameters of the most relevant research [23]. The algorithm normally can be implemented on a device such as Raspberry Pi, although a lot of researches focused on the optimization of FFT for the power consumption none tried to optimize FFT on the Raspberry Pi. Raspberry Pi is a single board micro-computer which can be programed and tasked to do all kinds of research, For the proposed work the Raspberry Pi was able to give us the same results as a fully functional computer, while most of the previous researchers worked on fully functional computers to get their results that is why the Raspberry Pi can be considered as a cost efficient device.

1.4 Research objectives

The Research objectives aim to use a reconfigurable Twiddle Factor to design a Fast Fourier Transform on the Raspberry Pi (RPi) hardware device. In the FFT multiplier there are a set of coefficients of fixed values these coefficients are referred to as the Twiddle Factor. The proposed work focuses on continuously optimizing the Twiddle Factor for getting as low power consumption as possible. A single and multiple-objective genetic algorithm are used to get the twiddle factor to the most optimum performance for both signal to noise ratio (SNR) and Switching Activity (SA). Summarizing the main objectives as follows:

1- To secure the SNR values by tasking SOGA with securing the SNR fitness function, lowering the Word Length of the Twiddle Factor of the Fast Fourier Transform by finding the most optimum solutions which meets the target goal for the SNR of being higher than 63dB observing the results of SNR each time.
2- To reduce the power by tasking MOGA with finding the SA values by finding the most optimum solutions which meets the target goals for SNR of being higher than 63dB and SA for being lower than 192 while lowering the word length of the Twiddle Factor and observing the results of SNR and SA each time.
3- To evaluate the optimization of SOGA and MOGA using different parameters such as Generation, Mutation and Crossover.

1.5 Research Scope

The research is limited to 32 bit, 16 points Radix-4 Single Path Delay Feedback (R4SDF) FFT structure on Radix-4. The coding for the FFT and the GA is in C# as well as using the Raspberry Pi. The results are limited to the comparison the proposed work on the RPi with previous work to reduce the power consumption of the word length. Single Objective Genetic Algorithm (SOGA) is tasked with finding the most optimum solutions for both SNR in which the value must be higher than 63dB, while Multi-Objective Genetic Algorithm is tasked with finding the most optimum values for both SNR and SA which are SNR higher than 63dB and SA lower than 192. Therefore, the procedure will continue by lowering the word length while the results of SOGA and MOGA are fulfilling the required goal values for both SNR and SA.

1.6 Organization of the Thesis

1- The thesis structure begins with the literature review in chapter 2. The Chapter 2 will discuss on FFT processor and the performance of FFT processor in terms of SNR and SA. Besides, it also contains the reviews in basic of Single Objectives GA follow by Multi Objectives GA method, review the advantages of Raspberry Pi, why choosing RPi and what are the other alternatives.

2- Chapter 3 is the methodology which will discuss about how the GA be implemented to optimize the FFT coefficient to obtain better SNR and SA values. The structure of the FFT and its performance will also be discussed.
3- Chapter 4 will discuss the results and findings of the research work for all three of the research objectives.
4- Finally, chapter 5 will conclude the research work and some future works are suggested.

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