LOW POWER FAST FOURIER TRANSFORM AND COMBINER OF MULTI CARRIER-CODE DIVISION MULTIPLE ACCESS RECEIVER SYSTEM FOR WIRELESS SENSOR NETWORKS

SITI LAILATUL BINTI MOHD HASSAN

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By

SITI LAILATUL BINTI MOHD HASSAN

Thesis submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

November 2019

DEDICATION

This thesis is dedicated to all my beloved family and friends, especially to my lovely kids Nisaa', Hana and Ahmad

Thank you for your endless love, sacrifices, prayers, supports and advice.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Doctor of Philosophy

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November 2019

Chairman : Associate Professor Nasri Sulaiman, PhD
Faculty : Engineering

This thesis presents a low power fast Fourier transforms (FFT) and combiner of multi-carrier code division multiple access (MC-CDMA) receiver for wireless sensor networks (WSN). WSN is a system comprises of sensor nodes with data sampling, data processing, and communication capabilities. In WSN, there is the need for scheduling of various communication activities between sensor nodes to the cluster-head or the neighbouring nodes. Most of the WSN adapt the time division multiple access (TDMA) and media access control (MAC) layer approach techniques for scheduling purposes. The main question was how to ensure the channel is most productive when the sensor nodes have the urge to transmit the data available but cannot because of the scheduling protocol adapted by the WSN. Besides, scheduling contributes to higher power consumption for sensor nodes in WSN, reducing the sensor nodes lifetime. This research is motivated by the desire to eliminate scheduling in the WSN communication protocol with low power MC-CDMA system designs. MC-CDMA offers a collision-free medium since MC-CDMA can process transmit or receive data simultaneously over a single communication channel. Most of the sensor nodes are battery operated and sometimes placed in an isolated area, making it difficult to change the battery or connect to a direct power supply. Thus, the design must be in low power for longer lifespan of the nodes. In this research, different point (16, 64, and 256-point) and radixes (radix-4 and radix-8) FFT module, and combiner module are considered and analysed. Integration of both modules forms the MC-CDMA receiver. Pipelined FFT function is to convert signal in the time domain to the frequency domain, while combiner performs de-spreading, channel estimation and data demodulation to recover the transmitted bits. The low power designs in MC-CDMA have been carried out using Verilog coding in Modelsim software, and the design verifications are done through Matlab. The design implementation is via Quartus and programmed on DE2-115 Altera field-programmable gate array (FPGA) board. Synopsys is used for power

and area consumption studies with 90nm CMOS Technology. The functionality analyses have been carried out on simulation, and the hardware implementation of the MC-CDMA receiver is tested to see the MC-CDMA receiver ability to received data without scheduling. Both simulation and hardware execution are successful where the receiver received and displayed the output accordingly. MC-CDMA achieves 39.13mW power consumption and 0.95mm^2 design area consumption. Signal-to-noise (SNR) module was implemented on the receiver, and the results show that average SNR for MC-CDMA receiver is above 31.92dB, good SNR result for wireless communication. The optimization process by removing all hierarchical design has reduced the power and area consumption with 59.61% power saving and 30.07% area saving. MC-CDMA implementation on FPGA board gave a total of 28.57mW power consumption and used 2,072/114,480 logic elements which are 2% of overall logic elements. In conclusion, MC-CDMA receiver design in this thesis is small, low in power, have good SNR value and the ability to eliminate scheduling, which is suitable for WSN sensor nodes processor.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

TRANSFORMASI FOURIER CEPAT DAN PENGGABUNG BERKUASA RENDAH DALAM SISTEM PENERIMA PEMBAWA PEMBAHAGIAN KOD PELBAGAI AKSES UNTUK RANGKAIAN PENDERIA TANPA WAYAR

Oleh

SITI LAILATUL BINTI MOHD HASSAN

November 2019

Pengerusi : Profesor Madya Nasri Sulaiman, PhD
Fakulti : Kejuruteraan

Tesis ini membentangkan tranformasi Fourier cepat (FFT) dan penggabung berkuasa rendah dalam sistem penerima pembawa pembahagian kod pelbagai akses (MC-CDMA) untuk rangkaian penderia tanpa wayar (WSN). WSN ialah system yang terdiri daripada nod-nod penderia dengan keupayaan pensempelan data, pemprosesan data dan komunikasi. Di dalam system WSN, terdapat keperluan penjadualan pelbagai aktiviti komunikasi antara nod penderia ke nod ketua kelompok atau nod-nod lain dalam kelompok sama. Kebanyakan WSN menggunakan teknik pembahagian masa pelbagai akses (TDMA) dan lapisan kawalan akses media (MAC) untuk tujuan penjadualan. Persoalan utama timbul daripada pemikiran bagaimana untuk memastikan penggunaan saluran yang paling produktif apabila nod penderia ingin menghantar data dengan segera tetapi terhalang dengan protocol penjadualan yang digunapakai oleh WSN. Selain itu, penjadualan menyumbang kepada penggunaan kuasa yang lebih tinggi untuk nod penderia dalam WSN, ini mengurangkan had usia nod penderia. Penyelidikan ini dimotivasikan oleh keinginan untuk menghapuskan penjadualan dalam protocol komunikasi WSN dengan sistem MC-CDMA berkuasa rendah. MC-CDMA menawarkan medium bebas perlanggaran kerana MC-CDMA mempunyai kebolehan memproses data terima dan hantar secara serentak melalui saluran komunikasi tunggal. Selain itu, kebanyakan nod penderia beroperasi dengan bateri dan kadang-kadang diletakkan di kawasan terpencil, menjadikan proses menukar bateri atau menyambung nod penderia ke bekalan kuasa adalah sukar dan hampir mustahil. Oleh itu, rekaan nod penderia mestilah berkuasa rendah untuk memastikan jangka hayat yang lebih panjang. Untuk mencapai matlamat ini, rekaan telah dijalankan menggunakan pengkod Verilog dalam perisian Modelsim dan pengesahan rekaan melalui perisian Matlab. Perlaksanaan perkakasan rekaan adalah melalui perisian Quartus pada papan bidang boleh program pelbagai pintu (FPGA) Altera DE2-115. Synopsys digunakan untuk

kajian kuasa dan kawasan cip dengan teknologi CMOS 90nm. Dalam penyelidikan ini, modul transformasi Fourier cepat (FFT) pelbagai size (16,64 dan 256) dan pelbagai radix (radix-4 dan radix-8) dan modul penggabung digunakan dan dianalisa. Integrasi kedua-dua modul ini akan membentuk penerima MC-CDMA. Fungsi FFT adalah untuk menukar isyarat dalam domain masa ke domain frekuensi, manakala penggabung melakukan pengumpulan data, menganggar saluran dan demodulasi data untuk memulihkan bit yang dihantar. Analisis fungsi telah dijalankan pada simulasi dan perkakasan penerima MC-CDMA untuk mengkaji keupayaan penerima MC-CDMA untuk menerima data tanpa penjadualan. Simulasi dan perkakasan berjaya dimana penerima MC-CDMA menerima dan memaparkan keputusan yang sepatutnya. Penerima MC-CDMA mencapai 39.13mW jumlah penggunaan kuasa dan 0.95mm2 jumlah penggunaan Kawasan. Modul nisbah isyarat-ke-bunyi (SNR) juga ditambah pada penerima MC-CDMA dan hasilnya menunjukkan secara purata penerima MC-CDMA mempunyai SNR sebanyak 31.92dB, nilai SNR yang baik utuk aplikasi tanpa wayar. Proses pengoptimuman dengan mengeluarkan reka bentuk hierarki telah mengurangkan penggunaan kuasa dan kawasan 59.61% penjimatan kuasa dan 30.07% penjimatan kawasan. Perlaksanaan MC-CDMA pada papan FPGA memberikan jumlah penggunan kuasa sebanyak 28.57mW dan menggunakan 2.072/114,480 elemen logik, hanya 2% dari jumlah keseluruhan elemen logik. Sebagai kesimpulan, reka bentuk penerima MC-CDMA di dalam tesis ini adalah kecil, berkuasa rendah, mempunyai nilai SNR yang baik dan keupayaan untuk menghapuskan perjadualan, ciri-ciri yang sesuai untuk pemproses nod sensor WSN.

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This thesis was submitted to the Senate of the Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

Nasri bin Sulaiman, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Haslina binti Jaafar, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Azilah binti Saparon, PhD
Associate Professor
Faculty of Electrical Engineering
Universiti Teknologi MARA
(Member)

Yusnani binti Mohd Yussoff, PhD
Senior Lecturer, Ir
Faculty of Electrical Engineering
Universiti Teknologi MARA
(Member)

ZALILAH MOHD SHARIFF, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date: 09 April 2020

Declaration by graduate student

I hereby confirm that:

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Name and Matric No: Siti Lailatul binti Mohd Hassan, GS41856

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This is to confirm that:

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Signature: _____
Name of Chairman of Supervisory Committee: Associate Professor Dr. Nasri bin Sulaiman

Signature: _____
Name of Member of Supervisory Committee: Dr. Haslina binti Jaafar

Signature: _____
Name of Member of Supervisory Committee: Associate Professor Dr. Azilah binti Saparon

Signature: _____
Name of Member of Supervisory Committee: Dr. Yusnani binti Mohd Yussoff

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LIST OF ABBREVIATIONS

acc	accumulator output
ACK	Acknowledge
ASIC	application-specific integrated circuit
BE	beacon-enable
BER	bit-error-rate
BMAC	berkeley media access control
CDMA	code-division multiple access
CPU	central processing unit
CSMA/CA	carrier sense multiple access/collision avoidance
CTS	clear to send
DAC	digital-to-analog converter
DARPA	defence advances research project agency
DFT	discrete Fourier transform
DI	data input imaginary
DIT	decimation-in-time
DIF	decimation-in-frequency
DR	data input real
DOI	data output imaginary
DOR	data output real
DS-CDMA	direct sequence code division multiple access
DS-MAC	dynamic sensor- media access control
DSN	distributed sensor network
DSP	digital signal processor

FIFO	first-in first-out
FFT	fast Fourier transform
FPGA	field-programmable gate array
FSM	finite state machine
GPS	global positioning system
HEX	Hexadecimal
IC	integrated circuit
IFFT	inverse fast Fourier transform
ISI	inter-symbol interference
MAC	media access control
MC-CDMA	multi-carrier code division multiple access
MCU	Microcontroller
MDC	multi-path delay commutator
MMP	mobility management plane
MMSE	minimum mean square error
MPU	Microprocessor
NAMA	node activation multiple access
np-CSMA	non-persistent carrier sense multiple access
OFDM	orthogonal frequency division multiplexing
PMP	power management plane
RAM	random access memory
RF	radio-frequency
ROM	read-only memory
RTS	request to send
S-MAC	sensor- media access control

SDF	single-path delay feedback
SNR	signal-to-noise ratio
SOSUS	sound surveillance system
SRAM	static random access memory
STDMA	spatial time division multiple access
SYNC	synchronization
T-MAC	timeout- media access control
TCP	transmission control protocol
TDMA	time division multiple access
TMP	task management plane
TRAMA	traffic-adaptive media access control
VHDL	very high-speed description language
WSN	wireless sensor network

CHAPTER 1

INTRODUCTION

1.1 Research Background

Wireless Sensor Networks (WSN) is a system consists of sensor nodes deployed over a geographical area [1]. These sensor nodes have the same essential function of data sampling, data processing, and communication capabilities to transmit and receive information [2]. WSN are widely used in environmental data collection, security monitoring, and sensor node tracking [3]. An architecture of a typical sensor nodes consists of four subsystems; power supply, sensing, processing, and communication subsystem [4].

Initially, sensor nodes will listen to the channel every time even when there is no data on the channel during the data aggregation, which creates idle listening, as the cluster-head or coordinator nodes do not know when data will be sent from its child nodes. Then, TDMA is presented, introducing the use of scheduling [5]. Scheduling removes the idle listening by creating a fixed time slot for transmitting and receiving for all nodes available in the system. This protocol saves energy by assigning the nodes to sleep modes every time the nodes finish transmitting or receiving data. It also saves battery life because the collision is avoidable; no retransmission is needed [6]. However, the difficulty with TDMA protocols is the synchronisation between nodes. The scheduling becomes more complicated when the topology changes either by insertion of new nodes, and nodes are off because of battery exhaustion, interference with the communication links and many other causes of increase or reduction of the number of nodes. It is difficult to change the slot assignment assigned in the first place since all nodes must agree on the slot assignments [7].

To avoid idle listening in the previous communication protocol and at the same time eliminating the scheduling problems, code-division multiple access (CDMA) protocols is considered as the best solutions [8]. CDMA offers a collision-free medium because sensor nodes can transmit or receive data simultaneously over a single communication channel. The introduction of MC-CDMA had enhanced the performance by reducing the computational complexity of CDMA. MC-CDMA is the hybrid of orthogonal frequency division multiplexing (OFDM) and CDMA techniques. It combines the advantages of both OFDM and CDMA to produce a spectrally, efficient multi-user access system [9]. MC-CDMA can process transmitted and received data in bulk. There is no more scheduling needed for WSN nodes to communicate with each other or cluster-head. It will improve the overall system reliability, and all data can be processed on a real-time basis, no more delays or data lost and fading along the way. This research is motivated by the desire to eliminate both idle listening and scheduling in the WSN communication protocol with low power design MC-CDMA systems.

This thesis aims to improve the performance of power, area and SNR of pipelined FFT, and combiner module for MC-CDMA receiver to eliminate the need for scheduling (particularly TDMA approach) in WSN communication. The pipelined FFT design must have ≤50mW power consumption and ≤1mm^2 area consumption. The combiner design needs to comply with ≤20mW power consumption and ≤0.5mm^2 area consumption. Overall, the MC-CDMA receiver design must achieve ≤50mW power consumption, ≤1mm^2 area consumption and ≥20dB SNR value for the best design to be implemented in the WSN system as sensor nodes required very low power and tiny processor for a longer lifespan.

1.2 Problem Statement

In WSN, there is a need for scheduling for various communication activities between sensor nodes to the cluster-head or the neighbouring nodes. Most of the WSN adapt the TDMA and MAC layer approach techniques for scheduling purposes [10]. The main question arises from the thought of how to ensure the channel is most productive when the sensor nodes fail to immediately transmit the data available because of the scheduling protocol adapted by the WSN. Scheduling is not an efficient protocol because it has the problem of allocating transmission segment to sensor nodes at each time and under different channel qualities. Three main reasons scheduling problem arise in WSN: the communication resources are shared amongst sensor nodes over a geographical area, during transmission, signals were interfered with each other, and some data may be lost due to impairments, such as fading and attenuation. Other problems related to scheduling are hidden nodes in the network, run time error, and real-time data communication[11]. All problems related to scheduling are tight to the major problems in WSN, which is the power consumption.

Power consumption is a major issue in WSN. Previous research in all WSN area; topology, routing, communication protocol, hardware and software implementation, highlights the importance of low power design [12]–[16]. In case of scheduling, power consumption increased when sensor nodes fail to send their data during their time segment, and it needs to retransmit. Sometimes, while waiting for their schedule to transmit, data have already been contaminated with noise, the need to retransmit again, causing more power consumption. In some other problem, it is not real-time data communication, making the available information useless, and this will be a waste of power [17].

The idea is to design an MC-CDMA receiver at which different sensor nodes can communicate simultaneously, without further coordination protocol and without worrying about when to transmit or receive. The MC-CDMA receiver will be able to successfully decode the simultaneous data receive and determine the source of the arrived data [18]. Since most of sensors nodes are battery operated and placed in an isolated area, MC-CDMA is the best choice for WSN sensor nodes processor because low power is a vital condition for its design. However, most of MC-CDMA research focuses on the signal-to-noise ratio (SNR), bit-error-rate

(BER) and behavioural analysis [19][20][21]. There is also a lack of studies of MC-CDMA in hardware implementation; which focused on power and area consumption. Most of the research on MC-CDMA with FPGA implementation only focus on its behaviour studies without concerning the power and area analysis [9][22][23][24]. Another gap in the studies of MC-CDMA is the application studies, where some of the research stops at the functionality analysis without applying them into real-world application [25].

MC-CDMA usually consists of two major blocks, which are the FFT and combiner. Although MC-CDMA is an ongoing study, there is a lack of research on utilizing the FFT and combiner blocks. Most of the MC-CDMA research focused on the SNR and BER without concerning the design architecture. There are a lot of FFT architectures studied by the previous researcher, for example, pipelined, memory, parallel, and many more [26][27][28]. This architecture can be implemented with various algorithms such as radix-2, radix-4, radix-8 and any larger radix value [29][30]. There are many types of research carried out on FFT; however, there is a deficient in the FFT application and implementation studies. Usually, the research stop at the software level, some manage to study up to hardware simulation; however, FFT had not been fully utilised in full system design [31]. This thesis overcomes all the related issues and studied the most common architecture use, which is pipelined with radix-4 and radix-8 configuration and the implementation of it in the hardware (FPGA).

In summary, this research suggests a total and comprehensive solution to eliminate the need for scheduling in the WSN using the low power MC-CDMA receiver implemented on FPGA, a well-known platform for low power, high design flexibility, and support parallel computing [19]. MC-CDMA allows the system to support multiple users (nodes communication) at the same time over the same frequency band, eliminating the scheduling problem. The MC-CDMA design adapted the low power consumption blocks such as pipelined FFT and combiner.

1.3 Objective

The contributions of this thesis are to improve the performance of power, area and SNR of pipelined FFT and combiner module for MC-CDMA receiver to eliminates the need for scheduling (particularly TDMA approach) in WSN communication.

In detail, the objectives of this research are:

1. To design and optimize low power FFT in MC-CDMA receiver with pipelined architecture and different radix and size configuration.

2. To optimize the combiner module in MC-CDMA receiver for hardware implementation.
3. To verify the performance of the MC-CDMA receiver in term of power, area, and accuracy.
4. To verify the functionality of the MC-CDMA receiver on FPGA for scheduling elimination.

1.4 Significance of the Study

The research proposes a new technique to be used in WSN using MC-CDMA to eliminate the scheduling problem in WSN. MC-CDMA architecture used in this research has low power consumption, low area consumption, and high accuracy. The MC-CDMA includes pipelined FFT in its design, and it is a well-known architecture for low power design.

The positive impacts of this research project are as follow:

i. Eliminates scheduling for data transmission in WSN without jeopardising power consumption.
ii. Our MC-CDMA design is low in power and very suitable to be implemented in WSN sensor nodes.
iii. Each data received by MC-CDMA receiver are easily segmented, and sender nodes are traceable.

1.5 Scope of the study

Scope of study in this research are as below:

- The MC-CDMA implementation is on the modulation/digital part of the receiver on the cluster-head nodes.
- The definition of WSN is for commercial use, open, and can be applied in various applications.
- FPGA board used in this research is Altera DE2-115 with Cyclone IV processor chip.
- 90nm technology library is used for power and area simulation using Synopsis.
- Three FFT sizes, 16, 64, and 256-point with two different configuration radix-4 and radix-8 are studied in this thesis.
- Matlab data are used as a benchmark for verification purpose.

1.6 Thesis Structure

The thesis is organised as per followings:

i. Chapter 1 is dedicated to the introduction of this thesis. It starts with a research background that includes the motivation for this research. Then, the description of problems and limitations of the existing approaches carried out by various researchers, followed by aims and research objectives of this thesis. Finally, the significance and scope of this research project were stated for further clarification.

ii. Chapter 2 presents the literature review for this thesis, which starts with an overview of WSN, followed by WSN architecture, WSN network communication architecture and also WSN network topology. Then, WSN applications are further discussed before the problems in WSN, and scheduling problems specifically are deliberated. Next, FFT algorithms and architectures were discussed, and previous processor type used in WSN are detailed out. Lastly, an overview of MC-CDMA, MC-CDMA receiver and transmitter as well as recent studies related to MC-CDMA on FPGA were presented.

iii. Chapter 3 covers the research methodology conducted throughout this research project. The chapter thoroughly discusses all the steps required to achieve all the objectives of this thesis, including pipelined FFT design, combiner and MC-CDMA design. Followed by designs validation process and also performance analysis in term of power, area, and accuracy.

iv. Chapter 4 describes in detail the contributions of this research to the field, which includes the low power pipelined FFT, low power combiner, and low power MC-CDMA design. This chapter also highlights the novelty of this research, which is scheduling elimination. This chapter extensively describes the experimental results along with the relevant and essential discussion on the advantages and limitations of the proposed design and implementation.

v. Chapter 5 summarizes the overall achievements and discoveries in this thesis and concludes the advantages and limitations of the works done. Finally, some potential improvements and suggestions are proposed for future research.

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