



UNIVERSITI PUTRA MALAYSIA

**MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING
STATIC SINGLE CELL FAULTS ON SRAM MEMORIES**

NOR AZURA ZAKRIA

FK 2013 142



**MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING
STATIC SINGLE CELL FAULTS ON SRAM MEMORIES**

By

NOR AZURA BINTI ZAKARIA

**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia,
in Fulfillment of the Requirements for the Degree of Master of Science**

August 2013

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DEDICATION

This thesis is dedicated to my beloved family;

Syed Al Firdaus Jamallulail B Syed Ahmad,

Sharifah Shahida Husna, Syed Mohd Nazim

and Sharifah Nurhana.

Appreciate your sacrifices.



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UPM

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

**MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING
STATIC SINGLE CELL FAULTS ON SRAM MEMORIES**

By

NOR AZURA BINTI ZAKARIA

August 2013

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Memory testing is a method that requires an algorithm capable of detecting faulty memory as comprehensively as possible to facilitate the efficient manufacture of fault free memory products. Therefore, the purpose of this thesis is to introduce a Data Background (DB) scheme to generate an optimal March Test Algorithm (MTA) for detecting faults of memory that are undetectable using existing algorithms. The present research focuses on two types of Static Single Cell Faults (SSCFs): Write Disturb Faults (WDFs) and Deceptive Read Destructive Faults (DRDFs). These faults are undetectable by existing algorithms with insufficient operation. To date, the main effort in this field of research is to improve fault detection by modifying or adding an operation sequence in the MTA. A relatively small number of test approaches have worked on the DB scheme instead of the MTA to improve fault coverage. However, these approaches were designed to improve the fault coverage for detectable faults only. Thus, the present research develops a new DB scheme to be applied to existing MTA to detect two WDFs and two DRDFs.

Two methods are proposed in this project. In Method 1, a multiple DBs generator with a bit-adjacent DB management scheme is applied for the selected MTA. This method is evaluated in terms of function and performance differences between the proposed MTA and existing MTA using the User Defined Algorithm (UDA) available in the MBISTArchitect tool. Findings show that both MTAs have the same testing time. However, the existing MTA of the Memory Built-In-Self Test (MBIST) required a bigger area overhead and consumed more power. Hence, Method 1 is not suitable to be used with the MBIST for System on Chip (SoC).

For Method 2, suitable solid DBs are used to provide higher fault coverage instead of using the existing MTA. The new MTA is defined by designing an automation program called DB generator. The DB generator computes all the possible DBs and filters the list of preferable DBs using efficient combination logic. The proposed MTA is obtained after the eliminating procedure of the preferable DB list using the SQ generation rule. Finally, the fault coverage will be calculated manually by doing fault evaluation analysis using Fault Primitives (FP) rules. Results show that WDFs and DRDFs are successfully detected with each proposed MTA. The proposed MTAs are also able to detect other SSCFs, such as Transition Fault, Stuck-At Fault, Incorrect Read Fault, Read Destructive Fault, and State Fault. Finally, based on the SQ generation rule, and the development of the DB generator, MTAs are generated. The present research demonstrates that the DB generator and proposed MTAs, such as March CL-1, March CI-2, March SR-1, and March SR-2, are successfully applied and designed, with up to 100% fault coverage.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

**SKIM LATAR BELAKANG DATA PELBAGAI DAN PADU UNTUK
MENGESAN KESALAHAN SEL TUNGGAL STATIK DALAM MEMORI
SRAM**

Oleh

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Ogos 2013

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Ujikaji memori merupakan teknik penting yang memerlukan algoritma yang baik bagi mengesan kesalahan memori dengan kadar liputan yang tinggi untuk menghasilkan produk memori tanpa kesalahan. Oleh itu, objektif tesis ini adalah memperkenalkan skim data yang bersesuaian untuk diguna pakai dalam Algoritma March (MTA) untuk mengesan dua jenis kesalahan sel tunggal statik memori iaitu kesalahan “Write Disturb Faults” (WDFs) dan “Deceptive Read Destructive Faults” (DRDFs). Hasil kerja penyelidikan sebelum ini, didapati MTA yang diperkenalkan gagal untuk mengesan kesalahan-kesalahan tersebut dalam masa ujian yang sesuai. Pelbagai usaha telah dibuat untuk meningkatkan kadar pengesanan kesalahan dengan kaedah mengubah atau menambah turutan operasi di dalam MTA. Tetapi kaedah ini tidak sesuai kerana ia akan meningkatkan masa ujian. Sebaliknya, terdapat beberapa penyelidikan terdahulu telah membuktikan dengan menggunakan skim latar belakang data (DB) di dalam MTA, kadar pengesanan kesalahan adalah tinggi dan penggunaan masa ujian yang pendek. Walau bagaimanapun, penyelidikan terdahulu hanya mengesan kesalahan konvensional sahaja. Oleh yang demikian, satu kajian susulan haruslah dibuat untuk menghasilkan kaedah baru dengan menghasilkan DB yang baru untuk mengatasi kelemahan algoritma.

Terdapat dua kaedah yang telah digunakan dalam projek ini. Dalam Kaedah 1, penjanaan pelbagai DB dilakukan dengan skim pengurusan DB pada MTA yang terpilih. Hasilnya, MTA yang dijana dengan DB baru berjaya mengesan kesalahan tersebut. Kaedah ini telah dinilai dari segi prestasi dan fungsi pada setiap MTA baru dan konvensional. Setiap MTA diperterjemahkan kepada perkakasan rekabentuk ujian dalaman memori (MBIST) dengan menggunakan perisian MBISTArchitect. Dari hasil penilaian, didapati kedua-dua simulasi mempunyai masa ujian yang sama.

Walau bagaimanapun, rekabentuk MBIST yang dihasilkan mempunyai saiz yang lebih besar dan penggunaan kuasa elektrik yang tinggi. Oleh itu, Kaedah 1 tidak sesuai untuk digunakan untuk system cip memori (SoC).

Bagi Kaedah 2, penghasilan DB padu (solid DB) yang sesuai di dalam MTA hendaklah digunakan untuk mencapai liputan pengesanan kesalahan yang lebih tinggi berbanding menggunakan MTA sedia ada. MTA baru dijana dengan bentuk program automasi dipanggil penjana DB. Penjana DB mengambil kira semua DB dan menapis senarai DB menggunakan gabungan logik yang cekap. Cadangan MTA diperoleh dengan mengikuti prosedur ujian yang dicadangkan menggunakan peraturan generasi SQ. Akhirnya, liputan kesalahan akan dikira secara manual dengan melakukan analisis penilaian kesalahan berpandukan peraturan Primitif Kerosakan Primitif (FP). Keputusan menunjukkan bahawa WDFs dan DRDFs berjaya dikesan dengan setiap penghasilan MTA. MTA yang dihasilkan juga dapat mengesan SSCFs lain, seperti "Transition Fault", "Stuck-At Fault", "Incorrect Read Fault", "Read Destructive Fault", and "State Fault". Hasil penyelidikan menunjukkan bahawa penjana DB dan MTA yang dicadangkan, seperti March CL-1, March CI-2, March SR-1, dan March SR-2, berjaya dijana dengan liputan kesalahan sehingga 100%.

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This thesis was submitted to the Senate of the Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

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TABLE OF CONTENTS

| | | Page |
|------------------------------|--|------|
| ABSTRACT | | i |
| ABSTRAK | | iii |
| ACKNOWLEDGEMENT | | v |
| APPROVAL | | vi |
| DECLARATION | | viii |
| LIST OF TABLES | | xiii |
| LIST OF FIGURES | | xv |
| LIST OF ABBREVIATIONS | | xvii |
| | | |
| CHAPTER | | |
| 1 | INTRODUCTION | 1 |
| | 1.1 Research Background | 1 |
| | 1.2 Problem Statement | 4 |
| | 1.3 Aim and Objective | 7 |
| | 1.4 Scope of Research | 7 |
| | 1.5 Project Contribution | 8 |
| | 1.6 Thesis Layout | 9 |
| | | |
| 2 | LITERATURE REVIEW | 10 |
| | 2.1 Introduction | 10 |
| | 2.2 VLSI Test Technology | 10 |
| | 2.3 The Design and Architecture of SRAM | 12 |
| | 2.4 Contemporary Memory Testing | 14 |
| | 2.5 SRAM Testing Methodology | 16 |
| | 2.5.1 March Test Algorithm | 16 |
| | 2.5.2 Memory Fault Taxonomy | 17 |
| | 2.5.2.1 Functional Fault Model and its Fault Notation | 17 |
| | 2.5.2.2 State Fault (SF) | 19 |
| | 2.5.2.3 Read Destructive Fault (RDF) | 19 |
| | 2.5.2.4 Stuck At Fault | 19 |
| | 2.5.2.5 Incorrect Read Fault (IRF) | 20 |
| | 2.5.2.6 Operation Detection of SF, RDF, STAF and IRF | 20 |
| | 2.5.2.7 Transition Fault (TF) | 20 |
| | 2.5.2.8 Write Destructive Fault (WDF) | 20 |
| | 2.5.2.9 Deceptive Read Destructive Fault (DRDF) | 21 |
| | 2.5.2.10 Write Destructive Coupling Faults (CFwds) | 21 |
| | 2.5.2.11 Deceptive Read Destructive Coupling Faults (CFdrds) | 21 |
| | 2.5.2.12 Transition Coupling Faults (CFtrs) | 21 |
| | 2.6 March Test Algorithm Generation and Previous Works | 22 |
| | 2.6.1 Early MTA Development | 22 |

| | | |
|----------|---|-----------|
| 2.6.2 | The Increased of Test Length in MTA | 22 |
| 2.6.3 | Multi Data Background in Memory Testing | 23 |
| 2.6.4 | Programmable Design to Generate MTA | 23 |
| 2.6.5 | Investigation of March Test Algorithm use for SSCFs Detection | 24 |
| 2.6.5.1 | Fault Analysis on MATS++ Algorithm (6N) | 24 |
| 2.6.5.2 | Fault Analysis on March C- Algorithm (10N) | 25 |
| 2.6.5.3 | Fault Analysis March SR Algorithm (14N) | 26 |
| 2.6.5.4 | Fault Analysis March CL Algorithm (12N) | 28 |
| 2.6.5.5 | Fault Detection Discussion | 29 |
| 2.7 | MBIST Implementation and the Strategy | 30 |
| 2.8 | Summary | 32 |
| 3 | RESEARCH METHODOLOGY AND EXPERIMENTAL RESULT OF METHOD 1 | 33 |
| 3.1 | Introduction | 33 |
| 3.2 | Test Procedure for Fault Detection | 33 |
| 3.3 | Research Methodology | 34 |
| 3.4 | Static and Dynamic Scheme in Memory Bit Adjacent Management | 36 |
| 3.5 | DBs Management in Bit-Oriented Test Memories | 38 |
| 3.6 | Hardware Implementation Flow | 39 |
| 3.7 | UDA Algorithm | 40 |
| 3.8 | Gate Level Synthesis Implementation Flow | 42 |
| 3.9 | Results and Discussion | 43 |
| 3.9.1 | New March Test Algorithm and its Fault Detection | 43 |
| 3.9.1.1 | Mod MATS++ (6N) | 43 |
| 3.9.1.2 | Mod March C- (10N) | 44 |
| 3.9.1.3 | Mod March CL (12N) | 44 |
| 3.9.1.4 | Mod March SR (14N) | 45 |
| 3.9.1.5 | Fault Coverage Comparison and Discussion | 47 |
| 3.9.2 | Implementation and Technical Evaluation on BIST Hardware | 47 |
| 3.9.2.1 | Cycle Testing Time | 48 |
| 3.9.2.2 | Correlation Area Overhead with Test Approaches | 49 |
| 3.9.2.3 | Correlation Power Performance with Test Approaches | 50 |
| 3.10 | Technical Drawback from the Result | 50 |
| 3.11 | Summary | 51 |
| 4 | METHODOLOGY AND EXPERIMENTAL RESULT OF METHOD 2 | 52 |
| 4.1 | Introduction | 52 |
| 4.2 | Data Background Generation Hardware | 52 |
| 4.3 | March Algorithm Generation | 54 |
| 4.4 | Results and Discussion | 56 |
| 4.4.1 | New MTA and its Detection | 56 |

| | | |
|----------|---|-----------|
| 4.4.1.1 | Modification of MATS++ and March C- | 56 |
| 4.4.1.2 | Modification of March CL with $W_n, =5$ | 56 |
| 4.4.1.3 | Modification of March SR with $W_n, =6$ | 61 |
| 4.4.2 | Technical Discussion on Generated MTA | 64 |
| 4.5 | Summary | 65 |
| 5 | CONCLUSION | 66 |
| 5.1 | Conclusion | 66 |
| 5.2 | Research Limitations | 66 |
| 5.3 | Tasks Achieved to Accomplish the Study Objectives | 67 |
| 5.4 | Suggestions and Future Work | 67 |
| | REFERENCES | 68 |
| | APPENDICES | 76 |
| | BIODATA OF STUDENT | 98 |
| | LIST OF PUBLICATIONS | 99 |

LIST OF TABLES

| Table | Page | |
|--------------|--|----|
| 1.1 | Fault Detection on Single Static Cell Faults by March Test | 5 |
| 1.2 | Test Approaches Using Various Types of DBs | 6 |
| 2.1 | Functional Fault Primitives | 19 |
| 2.2 | Detection Fault in MTA | 20 |
| 2.3 | MATS++ Algorithm (6N) | 24 |
| 2.4 | MATS ++ Operation and its Detection Analysis | 25 |
| 2.5 | March C- Algorithm (10N) | 25 |
| 2.6 | March C- Operation and its Detection Analysis | 26 |
| 2.7 | March SR Algorithm (14N) | 26 |
| 2.8 | March SR and its Detection Analysis | 27 |
| 2.9 | March CL Algorithm (12N) | 28 |
| 2.10 | March CL and its Detection Analysis | 28 |
| 2.11 | Faults Detection Summary by MTAs | 29 |
| 3.1 | Example of Possible DB in Bits Adjacent Management Scheme | 38 |
| 3.2 | New DBs Sequence in March SR | 45 |
| 3.3 | Fault detection Between Mod MTA with Its Conventional MTA | 47 |
| 3.4 | UDA Program of Selected March Test Algorithm 14N and 22N | 48 |
| 3.5 | Comparison of Cycle Testing Time | 48 |
| 3.6 | BIST Area Overhead Correlation with Existing Approach (March SR and March SS) and Proposed Approach (Mod March SR) | 49 |
| 3.7 | BIST Test Power Correlation with Existing Approach (March SR and March SS) and Proposed Approach (Mod March SR) | 50 |
| 4.1 | Example of the Possible Writing Sequence | 54 |
| 4.2 | New DB and New March CL | 58 |

| | | |
|-----|---------------------------------|----|
| 4.3 | Fault Detection by March CL-1 | 59 |
| 4.4 | Fault Detection by March CL-2 | 60 |
| 4.5 | New DB and new March SR | 62 |
| 4.6 | Fault Detection by March SR-1 | 63 |
| 4.7 | Fault Detection by March SR-2 | 64 |
| 4.8 | Fault Coverage of Generated MTA | 65 |



LIST OF FIGURES

| Figure | | Page |
|--------|--|------|
| 1.1 | Memory Dominance on Silicon (Schrader, 2005) | 1 |
| 1.2 | 2011 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)] (Executive Summary, 2011) | 2 |
| 1.3 | Example of a March Test (Van de Goor et al., p19, 1990) | 2 |
| 1.4 | Fault Classification | 3 |
| 1.5 | The Overview of the Flow for Generating the New MTA | 7 |
| 2.1 | On-chip Memory and Redundancy Growth Trend | 11 |
| 2.2 | The Architecture of SRAM – Block Diagram | 12 |
| 2.3 | 6T CMOS SRAM CELL | 13 |
| 2.4 | SRAM Cell Structure | 13 |
| 2.5 | Read and Write Circuitry | 14 |
| 2.6 | Memory Testing Terminology Development | 15 |
| 2.7 | SRAM Testing Overview | 16 |
| 2.8 | 9N Test Algorithm Concept and Data Retention Test | 17 |
| 3.1 | Flow Chart of the Research | 35 |
| 3.2 | Flow Chart of Static and Dynamic Scheme in Generating New MTAs | 37 |
| 3.3 | DBs Management in BOM | 38 |
| 3.4 | UDA Language Syntax | 41 |
| 3.5 | Hardware Implementation Process Flow using March Algorithm | 42 |
| 3.6 | Operation Sequence of WDF and DRDF Detection | 46 |
| 3.7 | Correlation of Test Length Operation (N) and SRAM Feature Due to the Testing Cycle Time | 49 |
| 4.1 | Flow Chart of DB Generator Design | 53 |
| 4.2 | Overall Architecture | 54 |

| | | |
|-----|--|----|
| 4.3 | Simulation Result of Generating DB for the case of $W_n=5$ | 57 |
| 4.4 | Simulation Result of Generating DB for the case of $W_n=6$ | 61 |



LIST OF ABBREVIATIONS

| | |
|----------------|---|
| <0/0> | Stuck At Zero notation |
| <0/1> | Stuck At One notation |
| ↑ | increasing address order |
| ↓ | decreasing address order |
| ↕ | arbitrary address order |
| BIST | Built In Self Test |
| BL | Bit Line |
| BLB | Complementary Bit Line |
| BOM | Bit Oriented Test Memories |
| CFdrds | Coupling Deceptive Destructive Faults |
| CFid | Coupling Idempotent Fault |
| CFin | Coupling Inversion Fault |
| CFst | Coupling State Faults |
| CFtrs | Coupling Transition Faults |
| CFwds | Coupling Write Disturb Faults |
| CMOS | Complementary Metal Oxide Semiconductor |
| DB | Data Background |
| DFT | Design for Testability |
| DPM | Defective Parts Per Million |
| DRAM | Dynamic Random Access Memories |
| DRDF< 0r0/1/0> | Deceptive Read Destructive Fault Zero |
| DRDF<1r1/0/1> | Deceptive Read Destructive Fault One |
| DRDFs | Deceptive Read Disturb Faults |
| DRT | Data Retention Test |

| | |
|---------------|--|
| FFMs | Functional Fault Models |
| FFPs | Functional Fault Primitives |
| FSMs | Finite State Machines |
| ICs | Integrated Circuits |
| IFA | Inductive Fault Analysis |
| IFA | Inductive Fault Analysis |
| IRF <r0/0/1> | Incorrect Read Fault Zero |
| IRF <r1/1/0> | Incorrect Read Fault One |
| IRFs | Incorrect Read Faults |
| ITRS | International Technology Roadmap for Semiconductor |
| LSI | Large Scale Integration |
| MBIST | Memory Built In Self Test |
| ME | March element |
| ME | March Element |
| MTA | March Test Algorithm |
| MUT | Memories Under Test |
| r0 | read 0 operation |
| R0 | reading operation |
| r1 | read 1 operation |
| RAM | Random Access Memories |
| RAMSES | Random Access Memory Simulator for Error Screening |
| RDF <0r0/1/1> | Read Destructive Fault Zero |
| RDF <1r1/0/0> | Read Destructive Fault One |
| RDFs | Read Disturb Faults |
| ROM | Read Only Memory |
| RTL | Register Transfer Level |

| | |
|--------------|--|
| S0 | State 0 |
| SAF0 | Stuck At Fault Zero |
| SAF1 | Stuck At Fault One |
| SAFs | Stuck At Faults |
| SDCFs | Static Double Cell Faults |
| SF <0/1/-> | State Fault One |
| SF <1/0/-> | State Fault Zero |
| SFs | State Faults |
| SoC | System On Chip |
| SOF | Stuck Open Fault |
| SQ | New Sequence of Writing Operations |
| SRAM | Static Random Access Memories |
| SSCFs | Static Single Cell Faults |
| TAGS | Test Algorithm Generation by Simulation |
| TF <↑/0> | Transition Up notation |
| TF <↓/1> | Transition Down notation |
| TFs | Transition Faults |
| TPG | Test Pattern Graph |
| TSMC | Taiwan Semiconductor Manufacturing Company |
| UDA | User Defined Algorithm |
| ULSI | Ultra Large Scale Integration |
| VDSM | Very Deep Submicron |
| VLSI | Very Large Scale Integration |
| w0 | write 0 operation |
| w1 | write 1 operation |
| WDF<0w0/1/-> | Write Destructive Fault Zero |

| | |
|--------------|-----------------------------|
| WDF<1w1/0/-> | Write Destructive Fault One |
| WDFs | Write Disturb Faults |
| WL | Word Line |
| WOM | Word Oriented Test Memories |



CHAPTER 1

INTRODUCTION

1.1 Research Background

Static Random Access Memory (SRAM) has become an indispensable component of digital systems. It is used for specified capabilities for standalone products or embedded memories in System on Chip (SoC) products. The number of SRAM cores used in SoC products is increasing dramatically because of the need to facilitate multiple applications simultaneously. Moreover, technology scaling will lead to smaller feature sizes while enabling a huge number of CMOS (Complementary Metal Oxide Semiconductor) transistors to be fabricated into a single chip (Wang et al., 2006). However, the smaller feature sizes of the transistor will increase the density of the cell array (Akashe et al., 2011), leading to the risk of unknown defects occurring in the memory cells (Fonseca et al., 2010).



Figure 1.1 : Memory Dominance on Silicon (Schrader, 2005)

It was reported by Schrader et al., (2005) that the memory component dominates the SoC by silicon area, as shown in Figure 1.1. Figure 1.2 (Executive Summary, 2011) shows that the function size, including memory size, is becoming smaller, thus increasing the likelihood of defect occurrence. Achieving a high memory yield requires understanding memory designs, modeling their faulty behaviors in the presence of defects, and designing adequate tests with minimum area overhead as well as efficient repair schemes (Hamdioui et al., 2004).

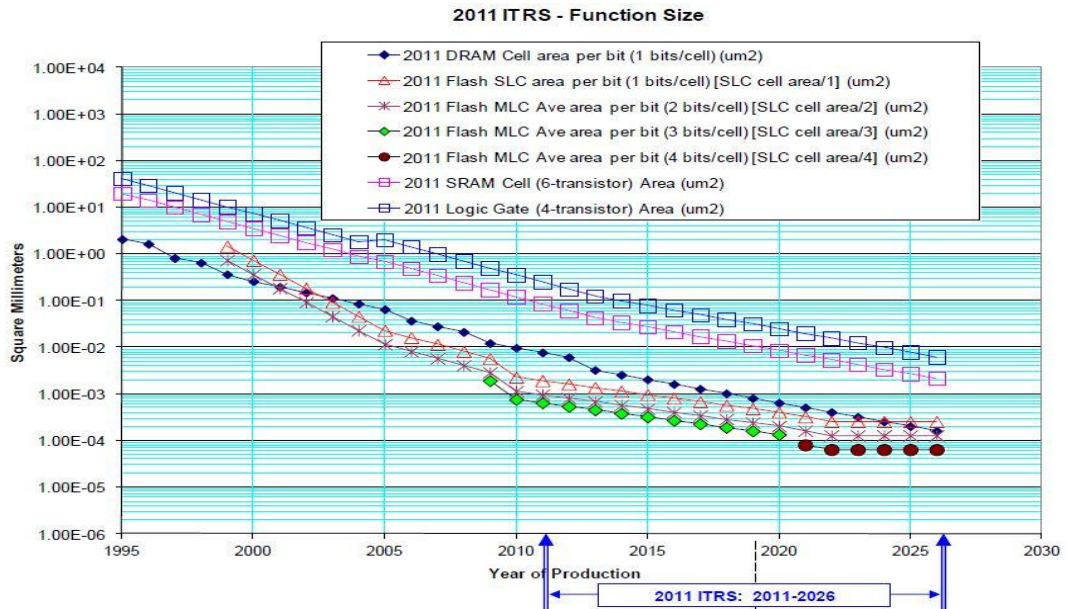


Figure 1.2 : 2011 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)] (Executive Summary, 2011)

In CMOS testing, defects occur due to the failure mode being prompted by the manifestation of a defect at the electrical level. Typically, failure modes are modeled as faults at the logic level abstraction of a physical defect. Fault abstractions or fault modeling provide the number of conditions that must be considered in deriving tests. To trace the substance of physical defect in memory testing, the test procedure is created based on the definition of the fault model (FM) described in fault primitives (FP).

```
(March element  $\uparrow$  (r0, w1))
for cell := 0 to n - 1 do
begin
read Memory[cell]; {expected value = 0};
write 1 to Memory[cell];
end;
{March element  $\downarrow$  (r1, w0)}
for cell := n - 1 downto 0 do
begin
read Memory[cell]; {expected value = 1};
write 0 to Memory[cell];
end;
```

Figure 1.3 : Example of a March Test (Van de Goor et al., p19, 1990)

Normally, embedded memory testing is tested by the developed a test algorithm known as a March Test Algorithm (MTA), as in Figure 1.3. Nair et al. (1978) first proposed an Algorithm Test Sequence to test stuck at fault physical defects with an optimum $4N$ test operation; later, Suk et al. (1981) proposed the MTA, with a $16N$ test procedure to test coupling faults. A detailed discussion of the MTA's operation in fault detection can be found in Chapter 3. Basically, an MTA is developed based on the test procedure; the MTA consists of a sequence set of March elements containing writing and reading operations. An example of the March element is described in Figure 1.3. An example of a March element is $(w0,r1)$, where 'w0' is writing a 0 into each cell and 'r1' is reading each cell with an expected 1 value. A memory cell is deemed faulty if the reading results show a 0 value. In Figure 1.3, the operation of " $\uparrow (r0, w1)$ " means reading a 0 and writing a 1 into the memory cell with an ascending address order from the lowest address to highest address. The operation of " $\downarrow (r1, w0)$ " means reading a 1 and writing a 0 into the memory cell with descending address order, ' \downarrow ' from the highest to the lowest address.

The test area can range in size from that appropriate for an LSI (Large Scale Integration) chip to that appropriate for an Ultra Large Scale Integration (ULSI) chip due to the rapid scaling of semiconductor devices. Therefore, the traditional test algorithms are no longer sufficient for testing various faults in standalone memories and embedded memories in SoC contexts. Thus, the development of efficient and effective testing procedures is essential to detect the defects that are expected to occur in SRAM.

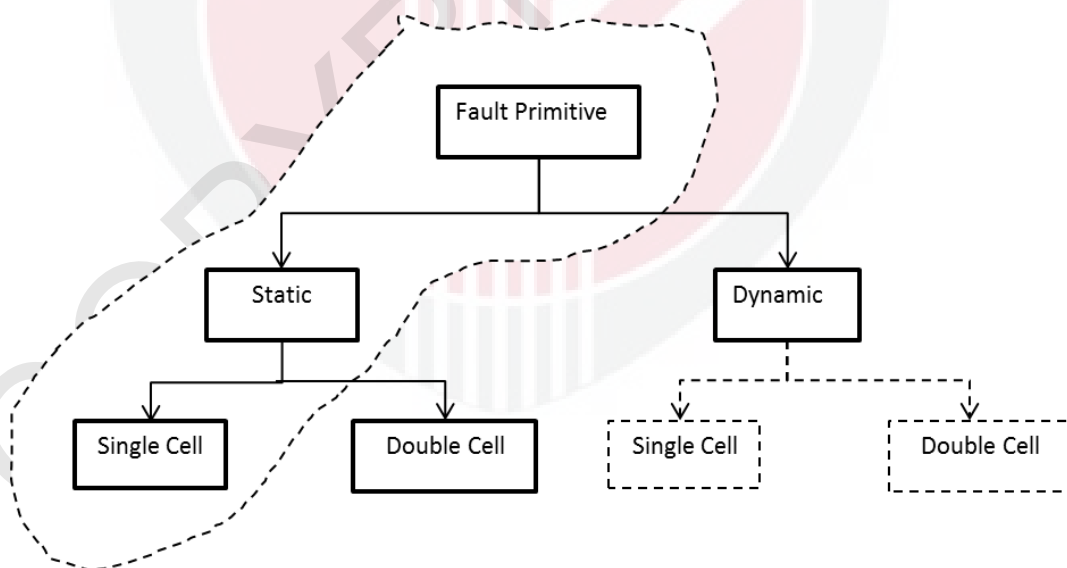


Figure 1.4 : Fault Classification

The CMOS process technology necessary for the dominant memories to be equipped into the ULSI silicon chip is under 180nm and below. SRAM testing under this process technology can be classified into two categories: dynamic and static faults (Figure 1.4). Static faults are FPs that sensitizes a fault by performing one operation; dynamic faults are FPs that performs more than one operation sequentially in order to sensitize a fault (Hamdioui et al., 2004). Until now, static faults have been a predominant fault class model of the memory cell, and numerous researches on the characteristics of static faults in CMOS memory and development of effective MTAs are still being conducted. Therefore, the focus of the present research, as highlighted in Figure 1.4, is to test Static Single Cell Faults (SSCFs). There are six types of SSCFs: Transition Faults (TFs), State Faults (SFs), Write Disturb Faults (WDFs), Read Disturb Faults (RDFs), Incorrect Read Faults (IRFs), and Deceptive Read Disturb Faults (DRDFs) (Van de Goor et al., 2000). The research conducted will also observe the detection of Static Double Cell Faults (SDCFs), such as Coupling Transition Faults (CFtr), Coupling Deceptive Destructive Faults (CFdrds), and Coupling Write Disturb Faults (CFwds) (Van de Goor et al., 2000).

1.2 Problem Statement

Over the years, the fault characterizations of ULSI chip fabrication in Very Deep Submicron (VDSM) CMOS process technology has become more challenging because of new faults arising that are not fully covered by the existing MTAs. Thus, the investigation of the SRAM testing approach involves functional fault models and MTA definition (Hamdioui et al., 2004). Therefore, in order to define the efficient MTAs required for VDSM technology, some problems need to be identified and addressed, such as undetectable static single cell faults (e.g., WDF and DRDF). Previously, these faults could not be detected by Van de Goor et al., (2000), Zordan et al., (2011), or Vardanian et al., (2002), as shown in Table 1.1. The undetected faults of WDF and DRDF have been tabulated in gray colored columns in the table.

Table 1.1 : Fault Detection on Single Static Cell Faults by March Test

| March Algorithm (Authors) | Fault Detection Results | | | | | | |
|---|-------------------------|-----|-----|-----|-----|------|-----|
| | SAF | SF | TF | WDF | RDF | DRDF | IRF |
| MATS+ (Van de Goor et al. (2002) and Zordan et al. (2011)) | 2/2 | 2/2 | 2/2 | 0/2 | 2/2 | 0/2 | 2/2 |
| March C- (Van de Goor et al. (2002) and Zordan et al. (2011)) | 2/2 | 2/2 | 2/2 | 0/2 | 2/2 | 0/2 | 2/2 |
| March SR (Van de Goor et al. (2002) and Zordan et al. (2011)) | 2/2 | 2/2 | 2/2 | 0/2 | 2/2 | 2/2 | 2/2 |
| March CL (Vardanian & Zorian, 2002) | 2/2 | 2/2 | 2/2 | 0/2 | 2/2 | 1/2 | 2/2 |

Table Notation:

0/2 – None of the faults are detected.

1/2 - One of the faults is detected.

2/2- Both faults are detected.

Each fault is divided into two types of faults; e.g., SAF is divided to SAF0 and SAF1.

From Table 1.1, it is shown that the MATS+(4N) and March C- (10N) algorithms failed to detect DRDFs and WDFs, March CL (12N) and March SR (14N) failed to detect WDFs, and March CL (12N) was only able to detect fault DRDFs faults. Based on the analysis, there are two assumptions can be made concerning how these shortcomings occur. One is that the faults cannot be detected due to the test sequence of the test algorithm's inability to fulfill its Functional Fault Primitives (FFPs) for both (Van de Goor and Al-Ars, 2002). The second is that the Data Background (DB) used in the MTA is inappropriate to detect the SRAM faults (Wu et al., 1999).

Weaknesses of an algorithm depend on the effectiveness of the operational test and operational data background set. An algorithm can be carried out in accordance with testing bit by bit, classified under Bit Oriented Test Memories (BOM), and testing word by word, classified under Word Oriented Test Memories (WOM) (Van de Goor et al., 1998). Effectiveness is achieved if an algorithm is said to have complete coverage for detecting faults in a short time rate (Wang et al., 2006; Wan Hassan et al., 2006). Shorter test times will reduce the cost of testing, resulting in low-cost production of the mass-manufactured chips (Hamdioui et al., 2000).

Previously, researchers have produced a number of improvements to MTAs by adding N operations to enable the testing of previously undetected faults (Hamdioui et al., 2002; Hamdioui et al., 2003; Vardanian et al., 2002; Harutyunyan et al., 2007; Harutyunyan et al., 2012; Hamdioui et al., 2002; Hamdioui et al., 2003; Vardanian et al., 2002; Harutyunyan et al., 2007; Zordan et al., 2011; Harutyunyan et al., 2012). By adding N operations, the test time will be increased, thus increasing test cost.

Table 1.2 : Test Approaches Using Various Types of DBs

| March Test Algorithm (Author) | Solid DBs | Multiple DBs | Conventional Fault (SF) | Improvement Coverage | Static Single Cell Fault | Coverage |
|--|-----------|-------------------------|-------------------------|----------------------|-------------------------------|---|
| RAMSES (Wu et al., 1999) | Yes | Yes (Varies up to 8 DB) | Yes (STAF, TF) | 100% | No | NIL |
| Data Background Generator (Wang et al., 2002) | Yes | No | Yes (STAF, TF) | 100% | No | NIL |
| Detecting Fault Under Bit Line Coupling (Irobi et al., 2010) | No | Yes | Yes | 100% | Yes (SF, DRDF, WDF, IRF, RDF) | 100% at March m-MSS but not March SR, March C-, or MATS++ |
| Proposed Method | Yes | Yes | Yes (STAF, TF) | 100% | Yes (SF, DRDF, WDF, IRF, RDF) | 100% |

The undetectable fault can also be solved by changing the DB operation in the test algorithm. Comparison between test approaches using various type of DBs in term of their fault detection improvement on conventional fault and SSCFs is tabulated in Table 1.2. Wu et al. (1999) developed the Random Access Memory Simulator for Error Screening (RAMSES) program to provide multi DB, consisting of eight DBs: P1 (0000), P2 (0101), P3 (0011), P4 (0110), P5 (0001), P6 (0010), P7 (0100), and P8 (1000). Wu et al. (1999) proved that by extending March C- and MATS++ with those DBs, the fault coverage is improved. Their designing of a data background generator to generate sequences of solid DBs (0s and 1s) proved to achieve up to 100% detection. However, the fault model covered in their works only conventional fault.

Irobi et al. (2010) proposed a new test algorithm, March m-MSS, which provided a solid-0 data background (00000000) , solid-1 data background (11111111), double-column stripes data background (00110011), double-column stripes data background (11001100), shifted double-column stripes data background (01100110) and shifted double-column stripes data background (10011001), which was able test all SSCF and SDCF faults under bit line coupling conditions. It was reported that using multiple DBs on March C-, March SR, and MATS+, the SSCFs are undetected with the condition of bit line coupling. Given these developments, it is necessary to develop

experiments to provide multiple DBs and to modify solid DBs to solve the undetectable issues.

1.3 Aim and Objective

The aim of the thesis is to improve the detection of SSCFs in existing MTAs to increase fault coverage. The main objectives of the proposed research can be summarized as follows:

To develop a test procedure consisting of sequence rules of DBs to detect the presently undetectable faults of SSCFs and SDCFs in the existing MTAs.

To provide a new method to modify DBs of the existing MTAs for obtaining better fault coverage and better hardware performance.

1.4 Scope of Research

The following items comprise the scope of this research:

The research involves generating multiple DBs and solid DBs after considering all possible DBs to test the conventional MTAs below 14N test length, such as MATS++ (9N), March C- (10N), March SR (14N), and Mod March CL (12N). Both methods are proposed to improve fault coverage of SSCFs. Figure 1.5 illustrates the flow of generating the new MTA based on the write operations numbers. DBs are filtered from all possible DBs following the test procedure rule. Those filtered DBs will be replaced by old DBs in the conventional MTA. Manual analysis to check the fault detection on each generated MTA will take place. The approach of this research is different compared to the approach based on the Address Fault Primitive and Test Pattern Graph used by Benso et al. (2005) and “Test Algorithm Generation by Simulation” used by Wu et al. (1999).

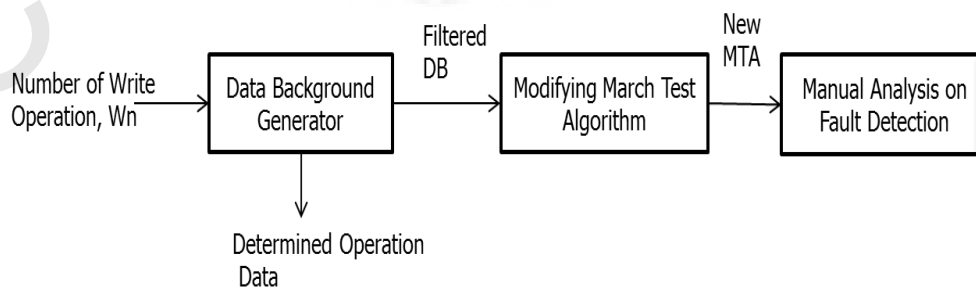


Figure 1.5 : The Overview of the Flow for Generating the New MTA

Method 1 manages the transition and non-transition at its bit-adjacent to memory word to generate managed DBs. There are two schemes included: a static scheme, whereby the data will write the same value twice, and a dynamic scheme whereby the new data will be written with the opposite values of the previous data.

The test evaluation of the specified MTA by Method 1 with static and dynamic scheme and MTA with solid DBs (0s and 1s) is conducted. The result of the generated MTAs will be compared in terms of its fault detection and Built-In-Self-Test (BIST) hardware performance with those with the conventional MTAs. The evaluation only picks one set of DBs per each Mod March SR (multiple DBs), March SR (solid DBs), and March SS (solid DBs) in the context of memory BIST. The testing scheme will be applied to single port and double port memories to evaluate the hardware performance in terms of hardware complexity, test cycle time, and test power.

Method 2 involves designing an automation program using Verilog HDL; it follows a proposition solution under the SQ generation rule to generate solid DBs. The flow in generating the possible DB follows the steps shown in Figure 1.5. Method 2 differs compared to the Method 1 only in terms of the rule used. Referring to the generated test patterns, the SQ rule will determine the final sequence bit pattern. The final bit test pattern will be used to generate the new MTA but will retain the sequence of the operation in the original MTA.

Since the rule on the proposed test procedure involves transition and a non-transition data, the solution will also observe the detection of SDCFs, especially CFtrs, CFwds, CFRds, and CFdrds.

Finally, based on the fault coverage and the hardware test evaluation results, the best method to be practiced in industry and research will be proposed.

1.5 Project Contribution

The test proposal consists of two methods to improve fault coverage in SSCFs detection as well as achieving low area overhead, test power, and test time by limiting the test length to $14N$ test operations. The following list briefly summarizes the main contributions of this dissertation:

A new method of bit adjacent management in BOM tests by practicing dynamic and static DBs to improve fault coverage of SSCFs.

A new method to generate a new MTA by generating a new sequence of DBs that follows the SQ generation rule to improve the fault coverage of SSCFs.

Designing data background generator follows the SQ generation rule. The design architecture is able to generate the optimum data background automatically with transition and non-transition operations to generate new MTAs.

1.6 Thesis Layout

The thesis is organized as follows:

In Chapter 1, the motivations of SRAM testing research are described, introducing the fundamental work of the importance of March Test Algorithm and its issues concerning test performance, including the problem statement, objectives, project contribution, research methodology and scope of the project.

Chapter 2 presents a detailed literature review of the relevant research work. Some of the analysis will take place in the context of highlighting the motivation of this research project. This chapter also explains the test fundamentals of the SRAM testing involved in the research work. The fault taxonomy of SSCFs and SDCFs are explained in detail. A summarized overview of SRAM testing that involves generating the FFM, FPs, and MTAs will be presented. The overview of the basic test algorithm elements and fault detection of each fault is discussed in detail.

Chapter 3 shows the research and methodology used in this research. The implementation of Method 1 and the overview of the development of the test algorithm, the proposed test procedure, the produced new MTA, and the result of fault detection is also discussed in detail. The MBIST implementation and the result in terms of area, test time, and test power are discussed in this chapter. A comparison of utilization of multiple DB and solid DB approach also takes place.

Chapter 4 discusses in detail the implementation of Method 2 based on the proposed SQ generation rule. The flow chart of designing the Data Background Generator and the generated DB results are presented. The produced MTAs and their fault detections are tabulated. Discussion of the results for the fault coverage and test power based on the produced MTA is also included in this chapter.

Chapter 5 summarizes research work and findings, also discussing research limitation and highlighting potential future work.

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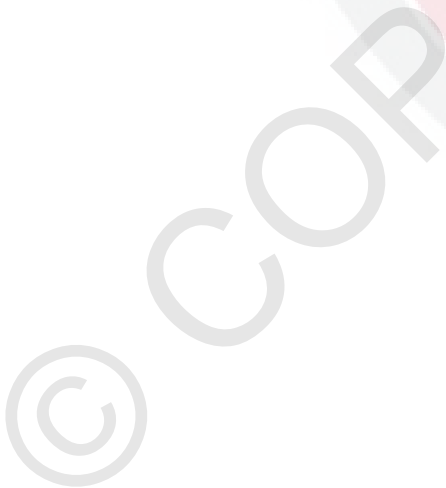
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Here her research focused on VLSI and memory testing and automation design development.

She has been published seven paper publications including 1 journal and 6 conference publications. She also been awarded of one patent with others pending.

LIST OF PUBLICATIONS

This research work presented in this thesis has yielded the following publications:

Zakaria, Nor Azura, W. Z. W. Hasan, I. A. Halin, R. M. Sidek, and Xiaoqing Wen.
"Testing Static Single Cell Faults using Static and Dynamic Data Background."
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"Fault Detection with Optimum March Test Algorithm" Intelligent Systems,
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"Fault Detection with Optimum March Test Algorithm." Journal of Theoretical
and Applied Information Technology, pp 018 – 027, Vol. 47. No. 1 2013



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