Optimization of fast fourier transform processor using genetic algorithm on Raspberry Pi

ABSTRACT

In many areas of engineering and science are widely using FFT processors in most of their applications, thus, the modern science requires continuously new optimizations which includes the FFT processor to have a lower power consumption and a smaller size. This paper revolves around the 16-point Radix-4 Single Path Delay Feedback (R4SDF) for optimizing the pipelined Fast Fourier Transform (FFT) processor, which can be done by using both Single Objective Genetic Algorithm (SOGA) and Multi-Objective Genetic Algorithm (MOGA), Signal to Noise Ratio (SNR) value which depends on the word length of the FFT processor, higher word length value of the FFT processor will result in a higher value for the SNR, Thus, this research aims to reduce the power consumption of the FFT processor by lowering the word length of Twiddle Factor for the FFT by using a SOGA to find the optimum results for SNR values while MOGA is set to find the optimum values for both SNR and SA while lowering the Word Length. Over the years the Genetic Algorithms (GA) proved to be one of the best methods for optimization. In this research the GA is for reducing the word length by optimizing its coefficients. The required amount of value for the SNR is to be more than 63 dB and less than 192 for SA. The proposed work was done successfully in optimizing the FFT by using SOGA to lower the word length until 12 bits and obtaining a SNR value of 66.452 which resulted in an improvement of 5.47% for SNR while MOGA was achieve a value of 65.033dB which provides (3.22%) improvement for the SNR and SA value of 140 which made reduction by (27%) for the SA.

Keyword: FFT processor; Genetic algorithm; Signal to noise ratio; Switching activity; SOGA; MOGA