Multi-bit error control coding with limited correction for high-performance and energy- efficient network on chip

ABSTRACT

In the presence of deep submicron noise, providing reliable and energy-efficient network on-chip operation is becoming a challenging objective. In this study, the authors propose a hybrid automatic repeat request (HARQ)-based coding scheme that simultaneously reduces the crosstalk induced bus delay and provides multi-bit error protection while achieving high-energy savings. This is achieved by calculating two-dimensional parities and duplicating all the bits, which provide single error correction and six errors detection. The error correction reduces the performance degradation caused by retransmissions, which when combined with voltage swing reduction, due to its high error detection, high-energy savings are achieved. The results show that the proposed scheme reduces the energy consumption up to 51.7% as compared with other schemes while achieving the target link reliability level. Also, it shows improved network performance as compared with ARQ-based scheme and close to forward error correction-based schemes.

Keyword: Crosstalk; Error correction codes; Automatic repeat request; Telecommunication network reliability; Forward error correction; Error correction; Delays; Hamming codes