A low quiescent current low dropout voltage regulator with self-compensation

ABSTRACT

This paper proposed a low quiescent current low-dropout voltage regulator (LDO) with self-compensation loop stability. This LDO is designed for Silicon-on-Chip (SoC) application without off-chip compensation capacitor. Worst case loop stability phenomenon happen when LDO output load current (Iload) is zero. The second pole frequency decreased tremendously towards unity-gain frequency (UGF) and compromise loop stability. To prevent this, additional current is needed to keep the output in low impedance in order to maintain second pole frequency. As Iload slowly increases, the unneeded additional current can be further reduced. This paper presents a circuit which performed self-reduction on this current by sensing the Iload. On top of that, a self-compensation circuit technique is proposed where loop stability is self-attained when Iload reduced below 100μA. In this technique, unity-gain frequency (UGF) will be decreaed and move away from second pole in order to attain loop stability. The decreased of UGF is done by reducing the total gain while maintaining the dominant pole frequency. This technique has also further reduced the total quiescent current and improved the LDO's efficiency. The proposed LDO exhibits low quiescent current 9.4μA and 17.7μA, at Iload zero and full load 100mA respectively. The supply voltage for this LDO is 1.2V with 200mV drop-out voltage. The design is validated using 0.13μm CMOS process technology.

Keyword: LDO; Low dropout regulator; Quiescent current; Self-compensation