UNIVERSITI PUTRA MALAYSIA

SIMULATION AND DEVELOPMENT OF UNIFIED POWER FLOW CONTROLLER USING MULTILEVEL INVERTER

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SIMULATION AND DEVELOPMENT OF UNIFIED POWER FLOW CONTROLLER USING MULTILEVEL INVERTER

By

NASHIREN FARZILAH BINTI MAILAH

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

January 2010
Dedicated to my parents, brothers, husband, and daughters
For with their prayers and loves, have given me strengths
Heavily loaded transmission lines and the inability to control the amount and direction of power flows have became major concerns to the power utilities. Some of the solutions taken by the power utilities are by expanding the size of power system network in terms of building new transmission lines, using higher rating equipments and installing more generating units. The power utilities also have improved the transmission lines capability and better utilizing of existing power system networks.

The power flows in the transmission lines in accordance to their series impedance, voltage magnitude at the sending end and receiving end, and phase angle between these two voltage ends. Electromechanically controlled devices have been used to control the power flow which is now steadily being replaced with static devices. The problem with these electromechanically controlled devices is sometimes they do not react fast enough especially during disturbances. Furthermore, they are subjected to wear and tear which requires regular monitoring and servicing.
The advancement in power electronics devices, which provide faster response compared to the electromechanical ones and require less maintenance as they do not wear and tear easily has attracted great interest from the researchers. Among these power electronics devices, Unified Power Flow Controller (UPFC) has gained a lot of attention due to its ability to control, simultaneously or selectively, all the three of power system parameters i.e. line impedance, voltage magnitude and phase angle.

In this work, UPFC’s simulation model has been designed and developed as a power system device to investigate the behaviour of the system under normal and abnormal conditions. A small-scale laboratory model has also been constructed to validate the findings obtained from the simulation model. To avoid high frequency components produced in Pulse Width Modulation (PWM), a 3-level Neutral Point Clamped (NPC) multilevel inverter has been proposed as the series inverter for the UPFC using Space Vector Modulation (SVM). The shunt inverter for UPFC is composed of a 6-pulse diode bridge rectifier and a line commutating thyristor bridge. A triggering circuit for the simulation model for the SSSC has been improved for Matlab/Simulink module. For the laboratory model, a switching circuit consists of PIC, optocouplers, IGBTs drivers and monostable multivibrators has been successfully constructed.

The proposed 3-level NPC inverter has been shown to have a better feature in terms of Total Harmonics Distortion (THD) with a simulation value of 13.36% $V_{LL}$ and experimental value of 15.65% $V_{LL}$. The THD value is lower compared to a similar work of 16.46%.
The additional voltage phase shift, $\phi$ produced by the SSSC has been shown to affect the phase shift between the sending end voltage and receiving end voltage. As the line impedance and both voltages are usually constant, any variation in phase shift between the two voltages will affect the amount of power flows in the transmission lines and its direction. The THDs of the voltage and current of the SSSC when connected between two busbars have been determined and a good agreement between the simulation and laboratory results has been achieved. From the simulation, the THD value of line voltage is approximately 1.3% which is lower compared to other work of 2.49% and 3.58%.

A comprehensive controllable UPFC using real power transfer algorithm and reactive power compensation algorithm has been successfully designed and constructed as a simulation model that is able to stabilize voltage with required power for fast changing loads.
Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

SIMULASI DAN PEMBANGUNAN PENGAWAL ALIRAN KUASA BERSATU MENGGUNAKAN PENYONGSANG BERBILANG ARAS

Oleh

NASHIREN FARZILAH BINTI MAILAH

Januari 2010

Pengerusi : Senan Mahmood Abdullah, PhD
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Talian penghantaran yang dibebani berlebihan dan ketidakbolehan mengawal jumlah dan arah pengaliran kuasa telah menjadi perhatian utama pengendali kuasa. Di antara penyelesaian yang diambil oleh pengendali kuasa adalah dengan memperbesarkan saiz rangkaian sistem kuasa dari segi membina tali...
 kepada haus dan lusuh di mana ia memerlukan pengawasan dan perkhidmatan yang teratur.

Kemajuan dalam peranti elektronik kuasa, di mana ia menyediakan tindakbalas yang lebih cepat berbanding peranti elektromekanikal dan memerlukan kurang penyelenggaraan kerana ia tidak haus and lusuh dengan mudah telah menarik banyak perhatian daripada penyelidik. Di antara peranti elektronik kuasa ini, Pengawal Aliran Kuasa Bersatu (PAKB) telah menarik banyak perhatian disebabkan oleh kebolehannya untuk mengawal, serentak atau memilih, kesemua tiga parameter sistem kuasa, iaitu galangan sesiri, magnitud voltan dan sudut fasa.

Di dalam kerja ini, model simulasi PAKB telah direka dan dibangunkan sebagai peranti sistem kuasa untuk menyelidik kelakuan sistem di dalam keadaan normal dan tidak normal. Sebuah model skala-kecil makmal juga telah dibina untuk mengesahkan penemuan yang diperolehi dari model simulasi. Untuk mengelak komponen frekuensi tinggi yang terhasil dalam modulasi denyut lebar (MDL), penyongsang berbilang aras 3-aras titik neutral terkapit (TNT) telah dicadangkan sebagai penyongsang sesiri bagi PAKB dengan menggunakan modulasi vektor ruang (MVR). Penyongsang pirau untuk PAKB terdiri daripada penerus jejambat diod 6-denyut and jejambat thyristor talian tukarterbit. Litar pemicuan bagi model simulasi SSSC telah ditambahbaikan untuk modul Matlab/Simulink. Bagi model makmal, litar pensuisan yang terdiri dari PIC, pengganding optik, pemacu IGBTs and pembilang getar monostabil telah berjaya dibina.
Penyongsang 3-aras TNT yang dicadangkan telah menunjukkan mempunyai sifat yang lebih baik dari segi nilai herotan harmonik seluruh (HHS) dengan nilai simulasi 13.36% $V_{LL}$ dan nilai ekperimen 15.65% $V_{LL}$. Nilai HHS ini adalah lebih rendah dibandingkan dengan kerja lain iaitu 16.48%.

Fasa berubah voltan tambahan, $\phi$ yang terhasil oleh SSSC telah ditunjukkan boleh mempengaruhi fasa anjakan di antara voltan hujung penghantaran dan voltan hujung penerimaan. Galangan sesiri dan kedua-dua voltan adalah tetap, mana-mana perubahan dalam fasa berubah di antara dua voltan akan mempengaruhi jumlah aliran kuasa dalam talian penghantaran dan arahnya. THD voltan dan arus SSSC apabila bersambung dengan dua busbar telah ditentukan dan persamaan yang baik telah diperolehi dari keputusan simulasi dan makmal. Dari simulasi, nilai HHS voltan talian adalah lebih kurang 1.3% yang mana ia lebih rendah apabila dibandingkan dengan kerja lain iaitu 2.49% dan 3.58%.

PAKB boleh kawal komprehensif menggunakan algoritma pindahan kuasa aktif dan algoritma penebusan kuasa reaktif telah berjaya direka dan dibina sebagai model simulasi yang boleh menstabilkan voltan dengan kuasa yang diperlukan untuk tindakbalas beban yang pantsa berubah.
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Last but not least, to my families, thank you for the prayers and encouragement that have given to me all these years and not forgetting my husband and daughters for their love and understanding.
I certify that a Thesis Examination Committee has met on 21 January 2010 to conduct the final examination of Nashiren Farzilah Binti Mailah on her thesis entitled "Simulation and Development of Unified Power Flow Controller using Multilevel Inverter" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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Date: 17 March 2010
DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institution.

__________________________
NASHIREN FARZILAH BINTI MAILAH

DATE : 25 JANUARY 2010
TABLE OF CONTENTS

DEDICATIONS ii
ABSTRACT iii
ABSTRAK vi
ACKNOWLEDGEMENTS ix
APPROVAL x
DECLARATION xii
LIST OF TABLES xvi
LIST OF FIGURES xviii
LIST OF ABBREVIATIONS xxiii

CHAPTER

1 INTRODUCTION
1.1 Background 1
1.2 Problem Statement 4
1.3 Aim and Objectives 6
1.4 Project Scope 7
1.5 Contributions 8
1.6 Thesis Layout 9

2 UNIFIED POWER FLOW CONTROLLER (UPFC)
2.1 Introduction 11
2.2 FACTS and UPFC 11
2.3 UPFC’s Construction and Principle of Operation 13
2.4 Operating Modes of UPFC 18
2.5 Control Modes of UPFC 20
2.6 Review of UPFC Previous Works 21
2.7 Summary 28

3 MULTILEVEL INVERTERS
3.1 Introduction 29
3.2 Multilevel Inverter 29
3.3 Neutral Point Clamped (NPC) Multilevel Inverter 32
3.4 Other Multilevel Inverter 35
3.4.1 Multi Point Clamped (MPC) Multilevel Inverter 36
3.4.2 Flying Capacitor (FC) Multilevel Inverter 37
3.4.3 H-bridge Cascaded Inverter 38
3.5 Control Strategies 40
3.5.1 Thyristor Commutation Techniques 41
3.5.2 Space-Vector Modulation (SVM) 42
3.6 Harmonics and Total Harmonics Distortion (THD) 46
3.7 Review of Multilevel Inverter Previous Works 46
3.8 Summary 53

4 METHODOLOGY OF SOFTWARE MODEL
4.1 Introduction 54
4.2 Design and Development of STATCOM 56
4.3 Design and Development of SSSC 64
4.4 Calculation of SSSC Conduction Angle 69
4.5 Design and Construction of Comprehensive Controller of Unified Power Flow Controller (UPFC)
  4.5.1 STATCOM’s Controller 76
  4.5.2 SSSC’s Controller 78
4.6 Summary 83

5 METHODOLOGY OF HARDWARE MODEL
5.1 Introduction 84
5.2 Design and Construction of STATCOM 84
5.3 Design and Construction of SSSC 86
5.4 Summary 99

6 RESULTS AND DISCUSSIONS
6.1 Introduction 101
6.2 STATCOM Results and Discussions 101
6.3 SSSC Results and Discussions 108
6.4 Comparison of SSSC Inverter : Simulation and Laboratory Models 113
6.5 Comparison with Others Works Regarding to Multilevel Inverter 118
6.6 Effect of Varying the Magnitude and Phase Angle of SSSC’s Additional Voltage, ΔV to the AC Power System
  6.6.1 Effect of Additional Voltage Magnitude, ΔV 120
  6.6.2 Effect of Additional Voltage Phase Shift, φ 124
6.7 Simulation of SSSC Connected Between 2 Busbars 128
6.8 Controllable UPFC Results and Discussions 131
  6.8.1 Full UPFC System with SSSC and STATCOM 132
  6.8.2 UPFC System with SSSC only 137
  6.8.3 UPFC System with STATCOM only 138
6.9 Summary 139

7 CONCLUSIONS
7.1 Conclusions 141

xiv
7.2 Future Works and Recommendations

<table>
<thead>
<tr>
<th>REFERENCES</th>
<th>APPENDICES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Appendix A1</td>
</tr>
<tr>
<td></td>
<td>Appendix A2</td>
</tr>
<tr>
<td></td>
<td>Appendix A3</td>
</tr>
<tr>
<td></td>
<td>Appendix B1</td>
</tr>
<tr>
<td></td>
<td>Appendix B2</td>
</tr>
</tbody>
</table>

| BIODATA OF STUDENT | 169 |
| LIST OF PUBLICATIONS | 170 |
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>3-level Neutral Point Clamped inverter output voltage levels and their switching states for phase A</td>
<td>34</td>
</tr>
<tr>
<td>3.2</td>
<td>Definition of switching states for 2-level</td>
<td>43</td>
</tr>
<tr>
<td>3.3</td>
<td>Space vectors, switching states and on state switches for 2-level</td>
<td>43</td>
</tr>
<tr>
<td>3.4</td>
<td>Definition of switching states for 3-level</td>
<td>44</td>
</tr>
<tr>
<td>3.5</td>
<td>Voltage vectors and switching states for 3-level</td>
<td>45</td>
</tr>
<tr>
<td>3.6</td>
<td>Compendium of the comparison</td>
<td>50</td>
</tr>
<tr>
<td>3.7</td>
<td>Comparison of multilevel inverters</td>
<td>50</td>
</tr>
<tr>
<td>3.8</td>
<td>Output voltage THD of a 5-level Diode Clamped inverter with various modulation method</td>
<td>51</td>
</tr>
<tr>
<td>3.9</td>
<td>Simulation and experimental results of line voltage THDs</td>
<td>52</td>
</tr>
<tr>
<td>6.1</td>
<td>Simulation results of harmonics spectrums and THDs of line-to-line voltage, line-to-neutral voltage and line current</td>
<td>117</td>
</tr>
<tr>
<td>6.2</td>
<td>Laboratory results of harmonics spectrums of line-to-line voltage, line-to-neutral voltage and line current</td>
<td>118</td>
</tr>
<tr>
<td>6.3</td>
<td>Laboratory results of line-to-line voltage, line-to-neutral voltage and line current THDs</td>
<td>118</td>
</tr>
<tr>
<td>6.4</td>
<td>Comparison of the proposed inverter model with other researcher’s inverter models</td>
<td>119</td>
</tr>
<tr>
<td>6.5</td>
<td>Simulation results of line-to-line voltage, $V_{LL2}$, line-to-neutral voltage, $V_{LN2}$ and line current, $I_L$ THDs of zero phase shift, $\phi$ for four different $</td>
<td>\Delta V</td>
</tr>
<tr>
<td>6.6</td>
<td>Laboratory results of line-to-line voltage, $V_{LL2}$ THD of zero phase shift, $\phi$ for four different magnitudes, $</td>
<td>\Delta V</td>
</tr>
<tr>
<td>6.7</td>
<td>Simulation results of line-to-line voltage, $V_{LL2}$, line-to-neutral voltage, $V_{LN2}$ and line current, $I_L$ THDs of 8.5V additional voltage, $</td>
<td>\Delta V</td>
</tr>
</tbody>
</table>
6.8 Laboratory results of line-to-line voltage, $V_{L1L2}$ THD of 8.5V additional voltage, $|\Delta V|$ for different phase shifts, $\phi$

6.9 THD value of line-to-line voltage, $V_{LL}$ and line current, $I_L$ for different phase shifts, $\phi$ when connecting SSSC between two busbars

6.10 Real and reactive powers with respect to phase shift, $\theta_{23}$ for $|\Delta V| = 10V$

6.11 Relationship between power, $P$ with the Additional Voltage Magnitude, $|\Delta V|$ and Additional Voltage Phase Shift, $\phi$ of the SSSC for full UPFC System
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Single line diagram of a UPFC</td>
<td>13</td>
</tr>
<tr>
<td>2.2</td>
<td>Shunt branch of the UPFC in inductive mode</td>
<td>15</td>
</tr>
<tr>
<td>2.3</td>
<td>Series branch of the UPFC</td>
<td>16</td>
</tr>
<tr>
<td>2.4</td>
<td>Vector diagram of UPFC power flow</td>
<td>18</td>
</tr>
<tr>
<td>2.5</td>
<td>Basic UPFC control functions</td>
<td>19</td>
</tr>
<tr>
<td>3.1</td>
<td>3-level Neutral Point Clamped inverter</td>
<td>34</td>
</tr>
<tr>
<td>3.2</td>
<td>5-level Multi Point Clamped inverter</td>
<td>36</td>
</tr>
<tr>
<td>3.3</td>
<td>5-level Flying Capacitor inverter</td>
<td>38</td>
</tr>
<tr>
<td>3.4</td>
<td>7-level H-bridge Cascade inverter</td>
<td>40</td>
</tr>
<tr>
<td>3.5</td>
<td>Classification of Multilevel Modulation Techniques</td>
<td>41</td>
</tr>
<tr>
<td>3.6</td>
<td>Space vector diagram for the 2-level inverter</td>
<td>44</td>
</tr>
<tr>
<td>3.7</td>
<td>Space vector diagram of the NPC inverter</td>
<td>45</td>
</tr>
<tr>
<td>4.1</td>
<td>Flow chart of overall project flow</td>
<td>55</td>
</tr>
<tr>
<td>4.2</td>
<td>Block diagram of a typical STATCOM</td>
<td>56</td>
</tr>
<tr>
<td>4.3</td>
<td>Block diagram and detailed representation of AC power supply</td>
<td>57</td>
</tr>
<tr>
<td>4.4</td>
<td>Detailed model of the rectifier section of the STATCOM</td>
<td>59</td>
</tr>
<tr>
<td>4.5</td>
<td>Detailed model of the inverter section of the STATCOM</td>
<td>59</td>
</tr>
<tr>
<td>4.6</td>
<td>Synchronizes 6-pulse generator for STATCOM</td>
<td>59</td>
</tr>
<tr>
<td>4.7</td>
<td>Complete schematic simulation model of STATCOM</td>
<td>61</td>
</tr>
<tr>
<td>4.8</td>
<td>Block diagram of a typical SSSC</td>
<td>65</td>
</tr>
<tr>
<td>4.9</td>
<td>Detailed model of the 3-phase, 3-level NPC SSSC</td>
<td>66</td>
</tr>
<tr>
<td>4.10</td>
<td>Complete schematic simulation model of SSSC</td>
<td>68</td>
</tr>
</tbody>
</table>
4.11 Conduction period determination for SSSC 70
4.12 Firing pulse generator of the SSSC 71
4.13 Output of firing pulses of the inner and outer SSSC 72
4.14 Complete schematic simulation model of controllable UPFC 73
4.15 Busbar voltage computation block 75
4.16 Busbar current computation block 75
4.17 Control block for STATCOM 77
4.18 Reactive power computation block 78
4.19 Vector diagram of relationship of $\theta_{23}$, with $|\Delta V|$ and $\phi$ 80
4.20 Control block for SSSC 81
4.21 Power demand computation block 82
4.22 Power transferred computation block 82
5.1 Block diagram of STATCOM laboratory model 85
5.2 Schematic diagram of STATCOM laboratory model 87
5.3 Block diagram of SSSC laboratory model 88
5.4 Schematic diagram of SSSC laboratory model 90
5.5 Schematic diagram of triggering circuit of SSSC laboratory model 92
5.6 Schematic diagram of power circuit of SSSC laboratory model 93
5.7 Flow chart of the triggering signals programming 95
5.8 Microcontroller programming without phase shift 97
5.9 Phase shift circuit 97
5.10 Microcontroller programming with phase shift 99
6.1 Laboratory setup of STATCOM 102
6.2 STATCOM power circuit

6.3 FC36M thyristor microcontroller triggering board

6.4 Waveform of the triggering signals and the thyristor’s voltage

6.5 Simulation results of single line A-to-neutral voltage and sag current without STATCOM

6.6 Laboratory result of single A-line-to-neutral voltage without STATCOM

6.7 Laboratory result of single line A-to-neutral sag current without STATCOM

6.8 Simulation result of single line A-to-neutral voltage and sag current with STATCOM

6.9 Laboratory result of single line A-to-neutral voltage with STATCOM

6.10 Laboratory result of single line A-to-neutral sag current with STATCOM

6.11 Simulation result of injected current supplied by STATCOM

6.12 DC capacitor voltage and DC capacitor current

6.13 Laboratory setup of SSSC

6.14 SSSC power circuit

6.15 SSSC switching circuit

6.16 Triggering signals from Port B and Port C

6.17 Phase different between inner IGBTs signal and outer IGBTs signal

6.18 Input and output optocoupler signals B1 and C1

6.19 Input and output driver signals B1 and C1

6.20 Phase shift signals from the phase shift circuit

6.21 Output waveform of B1 without phase shift with respect to AC supply signal
6.22 Output waveform of B1 with phase shift with respect to AC supply signal

6.23 Simulation model of 3-level NPC inverter with resistive load

6.24 Simulation result of SSSC with resistive load

6.25 Laboratory result of SSSC with resistive load

6.26 Comparison of 3-phase voltage of simulation and laboratory results

6.27 Harmonic contents of line-to-line voltage, line-to-neutral voltage and line current

6.28 Simulation model of the SSSC when connected to AC power system

6.29 Simulation results of voltage waveform of $V_1$ and $\Delta V$ at zero phase shift, $\phi$ for $|\Delta V|$ of 4.0V and 8.5V

6.30 Simulation results of voltage waveform of $V_1$ and $V_2$ at zero phase shift, $\phi$ for $|\Delta V|$ of 4.0V and 8.5V

6.31 Laboratory results of voltage waveform of $V_1$ and $\Delta V$ at zero phase shift, $\phi$ for $|\Delta V|$ of 4.0V and 8.5V

6.32 Laboratory results of voltage waveform of $V_1$ and $V_2$ at zero phase shift, $\phi$ for $|\Delta V|$ of 4.0V and 8.5V

6.33 Simulation results of voltage waveform for additional voltage phase shift, $\phi$ of 36° for $V_1$ and $\Delta V$, and $V_1$ and $V_2$

6.34 Simulation results of voltage waveform for additional voltage phase shift, $\phi$ of 72° for $V_1$ and $\Delta V$, and $V_1$ and $V_2$

6.35 Laboratory results of voltage waveform for additional voltage phase shift, $\phi$ of 36° for $V_1$ and $\Delta V$, and $V_1$ and $V_2$

6.36 Laboratory results of voltage waveform for additional voltage phase shift, $\phi$ of 72° for $V_1$ and $\Delta V$, and $V_1$ and $V_2$

6.37 Waveform of $V_1$, $V_2$ and $\Delta V$ for zero phase shift, $\phi$ with the 10V of additional voltage, $|\Delta V|$ 129

6.38 Waveform of $V_1$, $V_2$ and $\Delta V$ for 36° phase shift, $\phi$ with the 10V of additional voltage, $|\Delta V|$ 129
6.39 Waveform of $V_1$, $V_2$ and $\Delta V$ for 72° phase shift, $\phi$ with the 10V of additional voltage, $|\Delta V|$

6.40 Waveform of $V_1$, $V_2$ and $\Delta V$ for -36° phase shift, $\phi$ with the 10V of additional voltage, $|\Delta V|$

6.41 Waveform of $V_1$, $V_2$ and $\Delta V$ for -72° phase shift, $\phi$ with the 10V of additional voltage, $|\Delta V|$

6.42 Supply voltage and current for full UPFC system

6.43 Load current for full UPFC system

6.44 Real and reactive power at load for full UPFC system

6.45 Waveform of SSSC Voltage, Additional Voltage Magnitude and Additional Voltage Phase Shift for full UPFC system

6.46 Real and reactive power transferred by SSSC for full UPFC system

6.47 Waveform of System Voltage, STATCOM Voltage and STATCOM DC Voltage for full UPFC system

6.48 Busbar voltage at busbar $V_1$, $V_2$ and $V_3$, and the additional voltage by the SSSC, $\Delta V$ for full UPFC system

6.49 Real and reactive power transferred by SSSC with only SSSC in the system

6.50 Busbar voltage at busbar $V_1$, $V_2$ and $V_3$, and the additional voltage by the SSSC, $\Delta V$ with only SSSC in the system
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>AEP</td>
<td>American Electric Power</td>
</tr>
<tr>
<td>APOD</td>
<td>Alternative Phase Opposition Disposition</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>EPRI</td>
<td>Electric Power Research Institute</td>
</tr>
<tr>
<td>FACTS</td>
<td>Flexible Alternating Current Transmission Systems</td>
</tr>
<tr>
<td>FC</td>
<td>Flying Capacitor</td>
</tr>
<tr>
<td>GTO</td>
<td>Gate Turn Off</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>MDC</td>
<td>Modified-Diode-Clamped</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MPC</td>
<td>Multi Point Clamped</td>
</tr>
<tr>
<td>NPC</td>
<td>Neutral Point Clamped</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Disposition</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional Integral</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Lock Loop</td>
</tr>
<tr>
<td>PSC</td>
<td>Phase Shifted Carrier</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width-Modulation</td>
</tr>
<tr>
<td>SPWM</td>
<td>Sinusoidal Pulse-Width-Modulation</td>
</tr>
<tr>
<td>SSSSC</td>
<td>Static Synchronous Series Compensator</td>
</tr>
<tr>
<td>STATCOM</td>
<td>Static Synchronous Compensator</td>
</tr>
<tr>
<td>SVC</td>
<td>Static Var Compensator</td>
</tr>
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</table>

xxiii
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>SVM</td>
<td>Space Vector Modulation</td>
</tr>
<tr>
<td>TCSC</td>
<td>Thyristor Controlled Series Compensator</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonics Distortion</td>
</tr>
<tr>
<td>UPFC</td>
<td>Unified Power Flow Controller</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage Source Inverter</td>
</tr>
<tr>
<td>$V_1$</td>
<td>Generation voltage at busbar 1</td>
</tr>
<tr>
<td>$V_2$</td>
<td>Sending end voltage at busbar 2</td>
</tr>
<tr>
<td>$V_3$</td>
<td>Receiving end voltage at busbar 3</td>
</tr>
<tr>
<td>X</td>
<td>Series line impedance</td>
</tr>
<tr>
<td>$\Delta V$</td>
<td>Additional voltage</td>
</tr>
<tr>
<td>$</td>
<td>\Delta V</td>
</tr>
<tr>
<td>$\phi$</td>
<td>Additional voltage phase shift</td>
</tr>
<tr>
<td>$P_{23}$</td>
<td>Active power transferred between busbar 2 and 3</td>
</tr>
<tr>
<td>$Q_{23}$</td>
<td>Reactive power transferred between busbar 2 and 3</td>
</tr>
</tbody>
</table>