

FPGA implementation of handwritten number recognition using artificial neural network

ABSTRACT

Implementation of Deep Learning and Machine Learning Algorithms is always a challenge as they consume a lot of resources and power. In this paper, we have presented a very simple yet efficient way for creating an IP (intellectual property) core for Handwritten Number Recognition for FPGAs. The proposed ANN was verified and compared with several ANN networks on MATLAB, which gave the accuracy of about 99.38%. This network was implemented on Xilinx Zybo board XC7Z010CLG400-1. The total area covered by the IP block is 27.9%. The IP created is efficient and uses fewer resources thus suitable for other embedded applications.