UNIVERSITI PUTRA MALAYSIA

EFFICIENT HARDWARE DESIGN FOR PALM-DORSA VEIN IMAGE ENHANCEMENT

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

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May 2018

Chair : Abd. Rahman bin Ramli, PhD
Faculty : Engineering

Vein biometric system uses the pattern of veins in the human body as a unique identification. In this thesis, vein at palm-dorsa has been used as biometric modal. Nowadays, many researchers have developed numerous algorithms to enhance vein image for biometric purposes with most researchers focusing only on the use of software such as MATLAB or C language. The main problem with software implementation is that it cannot achieve the high computational speed required in specific application such as real time application that requires instant authentication. Hardware implementation can provide a solution to achieve real time performance. Recent hardware design implementations of vein image enhancement are not fast enough due to the inefficient hardware design architecture. The aim of this thesis is to develop hardware design for palm-dorsa vein image enhancement algorithm. The algorithm is designed in hardware using hardware description language for hardware realization. ModelSim-Altera has been used as hardware simulation platform. First, the vein image is applied with resample technique to remove the noise. Then, segmentation technique consisting of Difference of Gaussian and threshold are used to segment the veins. After that, median filter is used to remove noise introduced from the image segmentation. Finally, thinning technique is applied to get single line vein.

For hardware design of resample technique, parallel pipeline hardware has been developed to improve processing time and high throughput. It is designed to perform bicubic computation in parallel pipeline hardware to accommodate fast processing and high throughput with less hardware resources. For the interpolation process, instead of using multipliers, shifters are used to reduce hardware resources. For hardware design of Difference of Gaussian, one dimensional Gaussian technique that operated concurrently for first Gaussian filter and second Gaussian filter are implemented. For threshold, a simple comparator has been used to design threshold in hardware.

For hardware design of median filter, the improved moving windows hardware architecture has been developed. In the improved moving windows, instead of calculating all the pixels in the window, only certain pixels are calculated. The hardware design architecture of resample, segmentation and median filter also feature padding capability by reading the same address of memory as before for the padding pixel. For hardware design of thinning, parallel pipelined with Concurrent Condition Check Unit hardware architecture has been developed to enable the parallelism of the thinning algorithm. It contains modules that executed the thinning algorithm function simultaneously in hardware to speed up the process.

Finally, hardware design architecture of vein image enhancement algorithm has been proposed by integrating the hardware designs of resample, segmentation, median filter and thinning. The findings show that the proposed hardware design has the percentage of correct is about 98%. The proposed hardware design has the execution time of 8.5ms to 12.4ms depending on the thinning iterations. This work contributed in efficient hardware design architecture for palm-dorsa vein image enhancement for biometric purpose.

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REKA BENTUK PERKAKASAN YANG CEKAP UNTUK KEJELASAN IMEJ PEMBULUH DARAH BELAKANG TANGAN

Oleh

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Sistem biometrik pembuluh darah menggunakan imej corak pembuluh darah dalam tubuh manusia sebagai pengenalan unik. Dalam tesis ini, imej pembuluh darah pada belakang tangan telah digunakan sebagai modal biometrik. Pada masa kini, ramai penyelidik telah membangunkan banyak algoritma untuk meningkatkan kualiti imej pembuluh darah untuk tujuan biometric dengan kebanyakan penyelidik menumpukan kepada penggunaan perisian seperti MATLAB atau bahasa C. Masalah utama dengan pelaksanaan perisian adalah ia tidak dapat mencapai kecepatan pengiraan yang tinggi yang diperlukan dalam aplikasi tertentu seperti aplikasi waktu nyata yang memerlukan pengesahan segera. Pelaksanaan perkakasan dapat memberikan penyelesaian untuk mencapai prestasi waktu nyata. Pelaksanaan reka bentuk perkakasan untuk penambahbaikan imej urat baru-baru ini tidak cukup pantas kerana seni bina reka bentuk perkakasan yang tidak cekap. Objektif tesis ini adalah membangunkan reka bentuk perkakasan untuk algoritma penambahbaikan dan pembuluh darah belakang tangan. Algoritma ini direka bentuk dalam perkakasan menggunakan bahasa penerangan perkakasan untuk realisasi perkakasan. ModelSim-Altera telah digunakan sebagai platfom simulasi perkakasan. Permulaannya, imej pembuluh darah diterapkan dengan teknik persampelan semula untuk membuang hingar. Seterusnya, teknik segmentasi yang terdiri daripada Perbezaan *Gaussian* dan ambang digunakan untuk mensegmentasi pembuluh darah. Selepas itu, penapis median digunakan untuk membuang hingar yang dihasilkan daripada segmentasi imej. Akhir sekali, teknik penipisan digunakan untuk mendapatkan pembuluh darah garis tunggal.

Untuk reka bentuk perkakasan teknik persampelan semula, perkakasan talian paip selari telah dibangunkan untuk meningkatkan masa pemprosesan dan daya pemprosesan yang tinggi. Ia direka bentuk untuk melaksanakan pengiraan *bicubic* dalam perkakasan talian paip selari untuk memenuhi pemprosesan yang cepat dan daya pemprosesan yang tinggi dengan sumber perkakasan yang kurang. Untuk proses interpolasi, daripada menggunakan pendarab, penganjak digunakan untuk mengurangkan sumber perkakasan. Untuk reka bentuk perkakasan Perbezaan

Gaussian, teknik *Gaussian* satu dimensi yang beroperasi serentak untuk penapis *Gaussian* pertama dan penapis *Gaussian* kedua dilaksanakan. Untuk ambang, satu pembanding mudah telah digunakan untuk reka bentuk ambang dalam perkakasan.

Untuk reka bentuk perkakasan penapis median, seni bina perkakasan tingkap bergerak yang lebih baik telah dibangunkan. Dalam tingkap bergerak yang lebih baik, daripada mengira semua piksel dalam tetingkap, hanya piksel tertentu dikira. Seni bina reka bentuk perkakasan persampelan semula, segmentasi dan penapis median juga mempunyai keupayaan penebal dengan membaca alamat ingatan yang sama seperti sebelumnya untuk piksel penebal. Untuk reka bentuk perkakasan penipisan, seni bina perkakasan talian paip selari dengan Unit Semak Syarat Serentak telah dibangunkan untuk membolehkan keselarian algoritma penipisan. Ia mempunyai modul yang melaksanakan fungsi algoritma penipisan secara serentak dalam perkakasan untuk mempercepat proses.

Akhirnya, seni bina reka bentuk perkakasan algoritma penambahbaikan imej pembuluh darah telah dicadangkan dan dibangunkan dengan mengintegrasikan reka bentuk perkakasan persampelan semula, segmentasi, penapis median dan penipisan. Penemuan menunjukkan bahawa reka bentuk perkakasan yang dicadangkan mempunyai peratusan yang betul adalah kira-kira 98%. Reka bentuk perkakasan yang dicadangkan mempunyai masa pelaksanaan 8.5ms hingga 12.4ms bergantung kepada lelaran penipisan. Hasil kerja ini menyumbang kepada seni bina reka bentuk perkakasan yang cekap untuk penambahbaikan imej pembuluh darah belakang tangan untuk tujuan biometrik.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

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This is to confirm that:

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LIST OF ABBREVIATIONS

IR	Infrared
HDL	Hardware description language
LED	Light emitting diode
FIR	Far infrared
NIR	Near infrared
CLAHE	Contrast limited adaptive histogram equalization
LoG	Laplacian of Gaussian
DoG	Difference of Gaussian
DoG-HE	Difference of Gaussian-Histogram Equalization
FPGA	Field Programmable Gate Arrays
RTOS	Real Time Operating System
ROI	Region of interest
SoC	System on chip
DSP	Digital Signal Processor
TIP	Temporary interpolation point
FIFO	First in first out
PRCIA	Parallelized Row Column Interpolation Architecture
SRCIA	Serialized Row Column Interpolation Architecture
ALU	Arithmetic logic unit
DPRAM	Dual Port Block Memory
CCD	Charge-Coupled Device
CMOS	Complementary metal oxide semiconductor
DAC	Digital Analog Converter
ADC	Analog Digital Converter

ASIC	Application Specific Integrated Circuit
JPEG	Joint Photographic Experts Group
TIFF	Tagged Image File Format
RAM	Random access memory
VI	Vertical Interpolation
HI	Horizontal Interpolation
PSNR	Power signal to noise ratio
MSE	Mean squared error
GF3	3x3 Gaussian Filter
GF31	31x31 Gaussian Filter
CCCU	Concurrent Conditions Check Unit
s1	sample image 1
s2	sample image 2
s3	sample image 3
s4	sample image 4
s5	sample image 5
s6	sample image 6
s7	sample image 7
s8	sample image 8
s9	sample image 9
s10	sample image 10
s11	sample image 11
s12	sample image 12
s13	sample image 13

CHAPTER 1

INTRODUCTION

1.1 Background

Nowadays, security has become a primary concern for the public. So, biometric system is increasingly gain interest because the technology based on the uniqueness individual’s physical or behavioural characteristics. Vein biometric is emerging from other modality due to its strength and advantages.

Consumer devices including smartphones show increased interest in biometric system. One of the important things to consider in designing a biometric system for consumer electronic handheld devices is speed. Biometric technology uses complex and computation intensive image processing algorithms that require them to be implemented on powerful computers for acceptable processing time. However, handheld devices are usually constrained in resources and performance.

Vein biometric uses the vein pattern inside the human body as identification for further action such as authentication or access control. Different parts of the human body such as hands, palms, fingers and wrists can be used for this technology. Vein biometric uses infrared (IR) light generated from light emitting diodes (LED) to penetrate human skin. Due to the difference in absorption of blood vessels and other tissues, the reflected or transmitted IR light is captured by a sensor. The red blood cells present in the blood vessels absorb the IR light and form as darker image than the surrounding structure where the surrounding appears to be a brighter image as shown in Figure 1.1.

Vein image acquisition | **Infrared image** | **Vein image**

Figure 1.1: Vein image example (Palm Vein Recognition**).**

In the palm-dorsa vein biometric, the IR light from LED penetrates the skin, absorbed by red blood cell in the blood vessels and reflected to be captured by the sensor. The part where the IR light is absorbed or where the veins are, appear dark as shown in Figure 1.2.

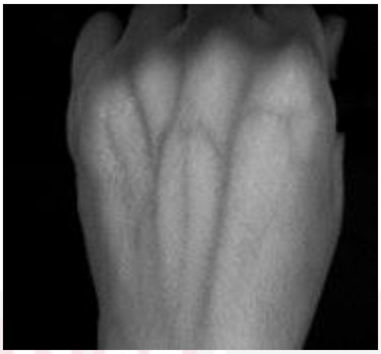

Figure 1.2: Palm-dorsa vein image example (Authentication Technologies**).**

After captured the vein image, it is processed by image processing techniques to extract the vein pattern. Various features information of the vein pattern such as branching points, thickness and so forth are extracted and stored as a template. The extracted vein pattern information is then stored as a template in the database for authentication purposes. Figure 1.3 shows the basic principle of the vein biometric.

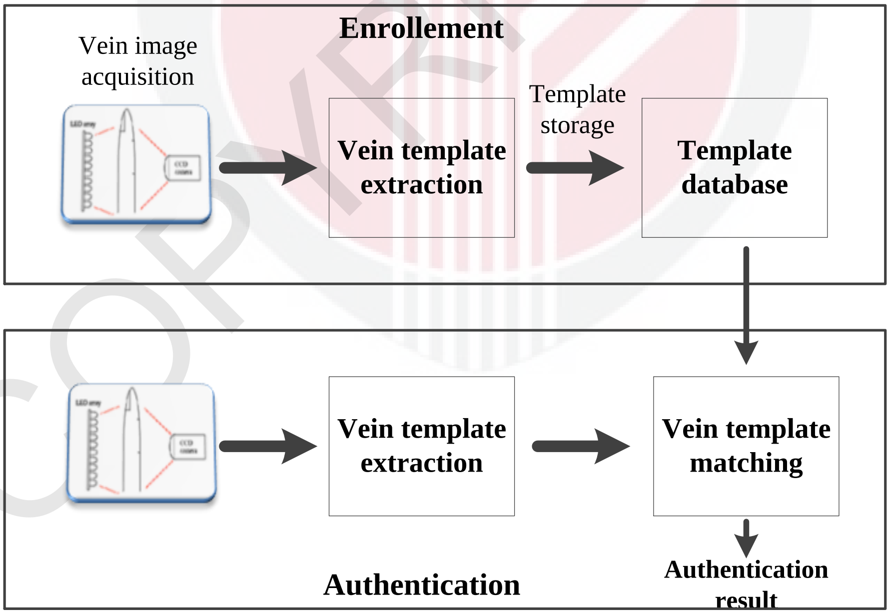

Figure 1.3: Vein biometric basic process.

Sensor or reader is used to acquire the vein image. Then authentication is processed using software on the computer or embedded system. However, software implementation of vein biometric cannot achieve high computation performance that is needed for real time applications. Hardware can provide solutions for higher performance. However, the hardware design of biometric system in hardware is challenging. Although few vein biometric hardware design have been proposed, there is still room for improvement especially in performance.

1.2 Problem Statements and Motivations

Fingerprint is a well-known biometric and is widely used because of the small device size. However, fingerprint biometric is less functional for work places such as construction sites due to the fact that certain fingerprints can be worn out. Hand geometry has excellent performance in usability but unfortunately it also has high false acceptance rate. Iris is good because it has low error rates but some users might feel psychological uncomfortable with light into their eyes. Furthermore, the iris recognition requires accurate eye position, causing the user to experience difficulty in providing this requirement every time. Whereas the vein can overcome all these weaknesses because the vein will not wear out or changes due to environment factor, contactless, offers hygienic and extremely difficult to forge.

Nowadays, many researchers have developed many algorithms to enhance veins for biometric. However, most researchers only focus on the use of software such as MATLAB or C language. The main critical problem of software implementation is that it cannot achieve high computation speed that is needed in specific application such as real time application that requires instant authentication. Hardware implementation can provide a solution to achieve real time performance. The hardware modules can be designed to accelerate performance of the vein enhancement algorithm. Pudzs *et al* (2013) and Khalil-Hani and Eng (2011) had implemented hardware design of their vein algorithm. However, performance result of 0.8 seconds for Pudzs *et al* (2013) and 0.5 seconds for Khalil-Hani and Eng (2011) are not fast enough. This is due to the inefficient hardware design architecture proposed by Pudzs *et al* (2013) and Khalil-Hani and Eng (2011) where the redundant process and hardware parallelism are not properly optimized. To cater for better performance, new hardware design architecture is needed to implement the vein image enhancement algorithm processing in hardware that is more efficient and faster.

For hardware design of bicubic interpolation, most hardware designs are burdensome memory with recurring memory access and redundant TIPs calculation. The TIPs have been calculated for an interpolation and then discarded. For the next interpolation process, the same memory addresses are read and the same TIPs need to be calculated. It's a waste of time, power and useless. Mahale *et al* (2014) had proposed a method to avoid repeated memory access and redundant TIPs calculations. However, the TIPs are stored in the Intermediate Buffer Bank and use large input buffer bank and output buffer bank that use more hardware resources. Therefore, an efficient hardware architecture that enables pipelining computation, excludes redundant calculation and reduce computation complexity is required.

For hardware design of Gaussian filter, Rao *et al* (2006), Zhang *et al* (2007), Khalil-Hani and Eng (2011), Joginipelly *et al* (2012), Song *et al* (2014) and Taibi *et al* (2015) have proposed hardware design architecture for Gaussian filter. However, the proposed filter size is small with the largest filter size is 15x15. For hardware design of Gaussian filter, it involves lot of calculations especially the larger mask filter size. For example, to perform a 5x5 Gaussian filter, there are 25 multiplications and 24 additions are involved in the calculation for each pixel. While to perform a 31x31 Gaussian filter, there are 961 multiplications and 960 additions are involved in the calculation for each pixel. The multiplication and addition operations increased drastically when the mask filter size increases. This requires large hardware resources to implement the Gaussian filter in hardware.

The same explanation applies to the hardware design of median filter. The proposed median filter size is small with the largest median filter size is 9x9. Larger median filter sizes involve many calculations due to the size of the filter. The calculation for small filter size is not so much, but for larger filter size a lot of calculations are involved, resulting in larger hardware resources required. For example, for 5x5 median filter, there are 25 pixels involved to determine the median pixel value. For 15x15 median filter, there are 225 pixels involved to determine the median pixel value. For 31x1 median filter, there are 961 pixels involved to determine the median pixel value. The calculations and hardware resources increased dramatically as the mask filter size increased. To cater this problem, a new technique and hardware design is needed to accommodate larger filter size, but less calculation involved.

While biometric as a technology has been around for decades, improvement for customer usability in term of speed of recognition is a major need. Ensuring biometric performance or customer experience is one way to develop biometric technology in line with market demand. In addition to concerns about privacy and security, researchers also need to focus on maximising user friendliness and more efficient and faster verification process. When developing the algorithm, the processes in the algorithm are considered whether can be processed in parallel on hardware due to parallelism capability in hardware is the key advantage to improve the performance of the algorithm. With the hardware design, faster verification process can be achieved.

1.3 Objectives

The aim of this research is to develop hardware design of vein image enhancement algorithm. In order to achieve the stated aim, the following objectives are being set as follows:

- To develop vein image enhancement algorithm using MATLAB and hardware designs of resample, Difference of Gaussian (DoG), median filter and thinning using hardware description language (HDL).
- To develop hardware design of the proposed vein image enhancement algorithm using hardware description language (HDL).
- To evaluate and to analysis the performance of the proposed hardware designs.

1.4 Scope of Works

In this thesis, the palm-dorsa vein image enhancement algorithm is developed using MATLAB. Then the hardware design of the algorithm is proposed and developed using Verilog Hardware Language Description. The hardware designs are developed individually for each technique. Designing of hardware is challenging due to hardware resource constraints and the complexity of hardware. When developing the hardware design, the processes in the algorithm are considered whether can be processed in parallel on hardware due to parallelism capability in hardware is the key advantage to improve the performance of the algorithm. Then using ModelSim-Altera, the designed hardware is simulated to verify the functionality. After that, each hardware designs are integrated to produce hardware design for the palm-dorsa vein enhancement algorithm. Functional verification is simulated to check the integration function.

The proposed hardware designs performance analyses are evaluated to assess the characteristics of the proposed hardware design. The proposed hardware designs have been compared with other state of the art techniques in hardware implementation for comparison compatibility. Furthermore, comparison of the proposed hardware designs performance with MATLAB are also evaluated for validity justification.

1.5 Thesis Contributions

This section summarizes the main contributions in this thesis. A more detailed discussion of the contributions is provided throughout this thesis. The main contributions are:

- A palm-dorsa vein image enhancement algorithm optimized for hardware is proposed. The algorithm enhances the vein image by removing noise and finally extracts the feature of the palm-dorsa vein image. The processes in the algorithm are considered whether can be processed in parallel on hardware because the parallelism capability in hardware is a major advantage to improve the performance of the algorithm.
- Hardware design architecture of resample is proposed. The proposed hardware design is an efficient architecture that enables pipelining computation with less hardware resource that excludes redundant calculation, reduce computation complexity and improve the throughput. For the interpolation process, instead of using multipliers, shifters are used to reduce hardware usage. Shift registers are used as an intermediate buffer between horizontal and vertical interpolation so that memory buffer or FIFO is not required. The hardware design architecture also features padding capability by reading the same address of memory as before for the padding pixel.
- Novel hardware design architecture of one dimensional Gaussian technique that operates concurrently for first Gaussian filter and second Gaussian filter is proposed. The hardware design architecture also features padding capability that comprises of coherent control unit that allowed the padding operation during data access.
- Novel hardware design architecture of median filter is proposed. The improved moving windows technique is proposed to accommodate larger median filter size which involves a lot of calculations due to filter size. In the

improved moving windows, instead of calculating all the pixels in the window, only certain pixels are calculated. The hardware design architecture also features padding capability that is implemented by reading the same address of memory location as before to provide padding image data.

- Parallel pipelined of moving window with Concurrent Conditions Check Unit (CCCU) hardware architecture is proposed to enable parallelism of the thinning algorithm.
- Novel hardware design architecture of palm-dorsa vein image enhancement algorithm is proposed. The main advantage of the proposed hardware design over other related works is a significantly faster performance than others. Since the proposed hardware design has the execution time of 8.5ms to 12.4ms, it is suitable for real time operation and handheld devices.

These contributions will be of broad use to the biometric system. However, these contributions may be applied to other. The contributions can contribute to a better and deeper understanding of hardware design architecture. This research provides an exciting opportunity to advance our knowledge of hardware design.

1.6 Thesis Organizations

This thesis is organized into five chapters including this chapter. Chapter 2 reviews the theories and related works to vein biometric technology. Different algorithm approaches for vein enhancement are also presented. The advantage and weakness of these approaches from prior works are discussed.

Chapter 3 presents the methodology behind the developed vein enhancement algorithm. First, the algorithm to enhance the vein is described in detail. After that the hardware design of the proposed vein enhancement algorithm is explained.

Chapter 4 presents the results and discussion of the proposed vein enhancement algorithm. These results are found from the experimental work from the MATLAB and the proposed hardware design of the vein enhancement algorithm. Then the performance evaluation of the proposed hardware design is presented and discussed. Chapter 5 concludes this research and discusses the possible future enhancements.

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