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FAST FOURIER TRANSFORM PROCESSOR IMPLEMENTATION FOR HIGH INPUTS ON FIELD PROGRAMMABLE GATES ARRAY

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By

ZAID ALI ABBAS

Thesis submitted to the School of Graduate Studies, Universiti Putra Malaysia, in fulfilment of the requirement for the Degree of Master of Science

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DEDICATION

I would like to dedicate my thesis to my beloved parents and my precious brothers for their endless support and care

Abstract of a thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

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August 2018

Chairman : Nasri bin Sulaiman, PhD
Faculty : Engineering

In the past few years, fast Fourier transform (FFT) proved to be an efficient method to accomplish the discrete Fourier transform (DFT) with less number of operations. FFT has been vastly applied for many applications, such as image processing technique, network data transmission (XDSL, WiMAX, and WLAN), orthogonal frequency-division multiplexing (OFDM), digital signal processing (DSP) and numerous applications that require high input data (1024 and up) processing. Low power and low complexity are the main concerns in high input FFT. Therefore, this research aims to investigate the power consumption, hardware resources usage and speed for radix-(2, 4 and 8) FFT processor, using the same device and environment to investigate the performance of each. Memory-based architecture chosen to use for FFT processors, due to the reduction in the number of butterflies and rotators, as they are reused for different stages of the FFT, were implemented on Cyclone II Field Programmable Gate Arrays (FPGA). Verilog Hardware Description Language (Verilog HDL) and VHDL Languages are used to program the algorithms into the FPGA. FFT algorithms will be implemented for up to 4096 points to measure the high load processing capability. The results show that for the 4096 points FFT, the radix-4 is the best trade-off in term of speed, resources and power consumption, which requires only 36% of the power required by the 4069 points radix-8 FFT and 58% of the power required by the 4069 points radix-2 FFT. On another hand, for the hardware resources, the result shows that the 4096 points radix-4 FFT used 30% of hardware resources furthermore; radix-8 FFT uses approximately 45%, in the meanwhile radix-2 require 20% only. For speed, the results shows that a 4096 points radix-4 FFT is 70% faster than 4096 points radix-2 FFT and 62% slower than 4096 points radix-8 FFT. While the radix-2 may be preferred, when it comes to power saving because it only need to consume 28% less

than radix-4 and 41% less than radix-8. Radix-8 is better when speed is the most important factor; it is notably 80% faster than radix-2 and 60% than radix-4.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

IMPLEMENTASI PEMPROSES TRASFORMASI FOURIER PANTAS BAGI INPUT TINGGI ATAS TATASUSUNAN LOGIK BOLEH ATURCARA MEDAN

Oleh

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Dalam beberapa tahun yang lalu, transformasi Fourier pantas (FFT) terbukti menjadi kaedah yang cekap dalam menyelesaikan transformasi Fourier diskret (DFT) dengan jumlah operasi yang rendah. FFT banyak digunakan dalam aplikasi, seperti teknik pemprosesan imej, penghantaran data rangkaian (XDSL, WiMAX, dan WLAN), pembahagian frekuensi orthogonal multipleks (OFDM), pemprosesan isyarat digital (DSP) dan pelbagai aplikasi yang memerlukan pemprosesan data input tinggi (1024 dan lebih tinggi).

Penggunaan kuasa dan saiz yang rendah adalah kepentingan utama dalam FFT input yang tinggi. Oleh itu, penyelidikan ini bertujuan untuk mengkaji penggunaan kuasa, penggunaan sumber perkakasan dan kelajuan untuk radix-(2, 4 dan 8) pemproses FFT menggunakan peranti dan persekitaran yang sama untuk menyiasat prestasi masing-masing. Senibina berasaskan memori yang dipilih untuk digunakan untuk pemproses FFT, disebabkan oleh pengurangan jumlah “kupu-kupu” dan rotator, kerana mereka digunakan semula untuk pelbagai peringkat FFT, telah dilaksanakan atas tatasusunan logik boleh aturcara medan Cyclone II, Bahasa Penerangan Perkakasan Verilog (Verilog HDL) dan Bahasa VHDL digunakan untuk memprogram algoritma ke atas FPGA. Algoritma FFT akan dilaksanakan sehingga 4096 mata untuk mengukur keupayaan pemprosesan beban tinggi.

Keputusan menunjukkan bahawa untuk 4096 mata FFT, radix-4 adalah terbaik dari segi kelajuan, sumber dan penggunaan kuasa, yang memerlukan hanya 36% daripada kuasa yang diperlukan oleh 4096 mata radix-8 FFT dan 58% daripada kuasa yang diperlukan oleh 4096 mata radix-2 FFT. Selain itu, bagi sumber perkakasan, keputusan menunjukkan bahawa 4096 mata radix-4 FFT menggunakan sumber perkakasan 30% yang digunakan oleh 4096 mata radix-8 FFT manakala radix-2 hanya memerlukan 20%. Dari segi kelajuan, hasil menunjukkan 4096 mata radix-4 FFT 70% lebih cepat daripada 4096 mata radix-2 FFT dan 62% lebih lambat daripada 4096 mata radix-8 FFT. Sedangkan radix-2 mungkin lebih diterima, apabila ia berkaitan dengan penjimatan kuasa kerana hanya memerlukan 28% kurang daripada radix-8 dan 41% kurang daripada radix-4. Radix-8 lebih baik apabila kelajuan adalah yang paling penting, terutamanya 80% lebih cepat daripada radix-2 dan 60% daripada radix-4.

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Last but not the least; I would like to thank my family, my parents and my brothers for supporting me spiritually throughout writing this thesis and my life in general

I certify that a Thesis Examination Committee has met on 1 August 2018 to conduct the final examination of Zaid Ali Abbas on his thesis entitled "Fast Fourier Transform Processor Implementation for High Inputs on Field Programmable Gates Array" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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This is to confirm that:

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LIST OF ABBREVIATIONS

ASIC	Application-Specific Integrated Circuit
CPU	Central Processing Unit
DFT	Discrete Fourier Transform
DIF	Decimation In Frequency
DIT	Decimation In Time
DSP	Digital Signal Processing
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Arrays
FSM	Finite State Machine
OFDM	Orthogonal Frequency Division Multiplexing

CHAPTER 1

INTRODUCTION

1.1 Background

Information was mainly delivered through the analog system in the past. However, advancement in digital signal processing has confirmed that many advantages regarding cost and performance are offered by technology over analog solutions. Discrete Fourier Transform (DFT) plays an important role in Orthogonal Frequency Division Multiplexing (OFDM) based communication systems in modern digital signal processing (DSP) and telecommunication(Chiueh & Tsai, 2008). The DFT is often used in linear filtering. A broad range of applications including video broadcasting, digital audio, the quantum mechanism(Ibrahim et al., 2016), image reconstruction(Jain, 1989), asymmetric digital subscriber loop (ADSL) has linear filtering. Rather unaffordable computation is needed by even the finite DFT signal to be completed. Specifically, N2 complex multiplications are required for DFT direct calculation of an input signal of length N. according to Colley and Tukey, fast Fourier transform (FFT) will be calculated in O (logrN) operations. In this operations, N refers to the length of the transform and r shows FFT decomposing radix(Cooley & Tukey, 1965; Saenz et al., 2015). In the field of Digital Signal Processing, FFT is regarded as a popular algorithm and is operated widely in digital communication particularly OFDM systems(S. He & Torkelson, 1998b; Oppenheim et al., 1989). The original contribution of Cooley and Tukey received considered attention and a large number of researchers attempt to extend and enhance their original work.

In many telecommunication systems and digital signal processing, FFT has become a key component. In OFDM, higher orders FFTs are needed for the purpose of increasing transmission efficiency. According to measuring storage system, higher data start with kilobyte (KB) equal to 1,024 bytes. The desire of consumer for high speed untethered access to multimedia together with entertainment services in recent years, has inspired and lead to wideband wireless communication system's growth(Daniels & Heath Jr, 2007). In physical layer of this standard, high throughput FFT/IFFT (Inverse fast Fourier transform) is considered as one of the main components which is indispensable for frequency-domain equalization together with orthogonal frequency division multiplexing modulation(Chiueh & Tsai, 2008). Different applications including video broadcasting, OFDM systems, speech processing, WLAN and image processing need high throughput FFT(Mookherjee et al.).

On the other hand, it is greatly used in the DSP field because of FPGA technology. Its architecture is flexible. It can be configured based on the project need of the user to calculate definite algorithms skillfully(Ibrahim et al., 2016). It is the best choice for FFT processors due to its low cost together with high capacity and performance. Traditionally, DSP chips or application Specific integrated circuits were utilized for design solutions. Nowadays, a great number of scholars shift to Field-programmable Gate Arrays (FPGA).

FPGA has different advantages over other technologies. They have the processing power for handling high-speed DSP. The capability of FPGA in performing repetitive operations in parallel propose a performance benefit to the instruction driven, DSP chips' sequential processing. They are a proper alternative to ASIC (Application-specific integrated circuit) due to their low-cost design cycles in comparison with ASIC which need large financial investments to be produced and updated. Moreover, unprecedented design flexibility is provided by them. Designers are provided with a platform in which they are able to assess their design decisions in terms of power, size, and throughput through their programmability(Wolf, 2004). Moreover, this feature enables them to get the most effective solution based on the system needs. The performance of FPGA is pushed upward because of advancement in the technology. Different improvements including implanted multipliers and RAM (Random-access memory) logic has lead to the simplification of the hardware implementation of DSP algorithm, which allows the digital information's transfer and transport.

1.2 Problem Statement

Fast Fourier Transform has been studied for a number of years. It has been used in various orthogonal frequency division multiplexing systems including IEEE 802.11ad standard for 60-GHz communication system is ratified(C. Wang et al.), terrestrial digital video broadcasting(K. Chen & Li, 2008; Saleh et al., 2013) and large number of mission information from/to users in real time like UAV (unmanned aerial vehicle)(Porcello, 2013). The outstanding features of these applications are the high inputs data.

For the seek of achieving efficient DFT, different FFT algorithms have been introduced. To achieve the required hardware resources and saving power in real-time applications, Different studies were conducted on the comparison of FFT algorithms, because the natural requirement of real-time applications is a hunger to high inputs data, however, there is no practical comparison between FFT algorithms in terms of high inputs.

To determine each algorithm (radix-2, radix-4, and radix-8) features under high inputs, and determine the best among these algorithms; this is done by measuring the system power, speed and hardware resource consumption.

In order to manage the parameters boundaries, a certain consideration should be counted such as the amount of data limitations. Furthermore, any amount of data above 1024 considered high input data. This kind of parameters limits the system performance especially when these parameters are measured such as speed, system power consumption, and hardware complexity.

1.3 Objectives of the research

Designing an efficient FFT processor for high inputs is the main objective of this research. The following steps are proposed to achieve this objective:

1- To design Radix-2, Radix-4, and Radix-8 memory based FFT algorithms on FPGA to examine the performance of high inputs data in terms of processor speed, power consumption, and hardware complexity.
2- To investigate the most efficient FFT algorithm using FPGA processor that offers the best performance in terms of speed, resources, and power consumption.
3- Identify the suitable systems required for the FFT algorithms and the suitable size for these systems.

1.4 Research scope

In this research, FFT processors will be designed based on memory-based architecture. However, the research will not propose new algorithms, rather compare the existing one, and implement them on FPGA. Any FFT can be perform in three stages. First stage decompose an N point time domain signal into N signals each containing a single point, second stage, find the spectrum of each of the N point signals. Finally, synthesize the N frequency spectra into single frequency spectrum. Figure shows the FFT flow diagram(Smith, 1997).

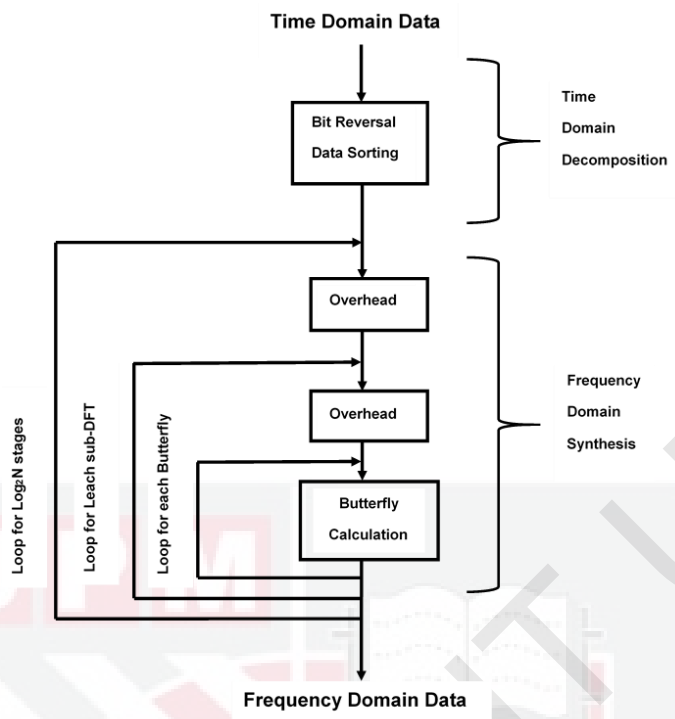

Figure 1.1 : FFT flow diagram(Smith, 1997)

Based on literature, most of the results for other researcher in the same filed, the power consumption range between (26) to (535) mWatts for the same number of points (4096). Meanwhile speed results range between (4093) to (150000) cycles. For hardware usage, it hard to specific certain range due to the vast of technologies been used to implement the algorithms from one researcher to others.

The FFT processors designed for up to 4096 points. The word lengths applied are 16-bit and 8-bit for input data. The twiddle elements used 16-bit because twiddle factor length must be less than or equal to input data lengths.

The speed of the processor is set to 50 MHZ, which is the maximum level of the Altera DE2C70 FPGA frequency. Since no external clocks are operated, FPGA PLLs are not used.

System's accuracy is measured through hardware implementation for real results. The power is precisely calculated from algorithm operations. The power's amount for operation is measured separately through applying Altera power function for accurate findings.

1.5 Thesis Outlines

This research consists of five chapters including:

Chapter 1: This chapter discusses the general background to the field of study following by discussion on problem statement and research objectives to solve the research problem. Finally, the scope of the study is discussed.

Chapter 2: This chapter reviews the existing literature on the field of study. FFT architecture together with FFT algorithm will be discussed in this chapter.

Chapter 3: the used methodology to address the research objectives of the study will be discussed in this chapter. It will begin with designing the FFT processor. Then, the FFT algorithms will be validated and implemented on the processor for various N-point values. Finally, the FFT output values are verified for deciding whether the system is working properly or not.

Chapter 4: discussion of the results and findings of the study will be presented in this chapter.

Chapter5: conclusion on the findings of the study together with some suggestion for future works will be discussed in this chapter.

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