

Signal-to-noise ratio study on pipelined fast fourier transform processor

ABSTRACT

Fast Fourier transform (FFT) processor is a prevailing tool in converting signal in time domain to frequency domain. This paper provides signal-to-noise ratio (SNR) study on 16-point pipelined FFT processor implemented on field-programable gate array (FPGA). This processor can be used in vast digital signal applications such as wireless sensor network, digital video broadcasting and many more. These applications require accuracy in their data communication part, that is why SNR is an important analysis. SNR is a measure of signal strength relative to noise. The measurement is usually in decibels (dB). Previously, SNR studies have been carried out in software simulation, for example in Matlab. However, in this paper, pipelined FFT and SNR modules are developed in hardware form. SNR module is designed in Modelsim using Verilog code before implemented on FPGA board. The SNR module is connected directly to the output of the pipelined FFT module. Three different pipelined FFT with different architectures were studied. The result shows that SNR for radix-8 and R4SDC FFT architecture design are above 40dB, which represent a very excellent signal. SNR module on the FPGA and the SNR results of different pipelined FFT architecture can be consider as the novelty of this paper.

Keyword: FPGA; Pipelined FFT; Radix-4; Radix-8; SNR