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DEVELOPMENT OF LOW POWER VITERBI DECODER ON COMPLEX PROGRAMMABLE LOGIC DEVICE PLATFORM

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By

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Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Doctor of Philosophy

DEVELOPMENT OF LOW POWER VITERBI DECODER ON COMPLEX PROGRAMMABLE LOGIC DEVICE PLATFORM

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March 2018

Chairman : Associate Professor Noor Izzri Abdul Wahab, PhD, PEng, CEng
Faculty : Engineering

Space Time Trellis Code (STTC) and Viterbi algorithm combinations are known to offer a robust forward error correction system. This especially has been used in a noisy digital communication system such as wireless communication. A traditional Viterbi decoder would contain three main units; Branch Metric Computation Unit (BMC), Add Compare Select Unit (ACS) and path metric updater (PMU). This combination of STTC and Viterbi algorithm however will cause a complexity in STTC decoder and increase power consumption of the system in addition to reducing battery life of portable devices. The objectives of this study are to analyse high power consumption in the STTC Viterbi decoder, design low complexity model of the ACS and the PMU for STTC Viterbi decoder and develop low power 0.18µm CMOS Viterbi decoder for STTC. For the decoder, maximum likelihood sequence estimation (MLSE) method has been used in the proposed Viterbi decoder in order to find the highest probability that is selected from all possible transmitted bit sequences which are nearest to the received sequences. ACS and PMU have been reported in previous findings to consume most power of decoder. This thesis thus proposes suitable methods to reduce power consumption in Viterbi decoder by enhancing the ACS and PMU module. For ACS, the traditional method of Viterbi algorithm is to add the previous state metric with the current branch metric, compare the new branch metric and select the minimum branch metric. This thesis however proposes to remove the "Add" function in this Viterbi algorithm by comparing the minimum value of branch metric from the four states of branch metrics, selecting the minimum values and encoding the minimum branch metrics. For the path metric updater unit (PMU), the traditional method of Viterbi algorithm is to store the selected minimum value of branch metric in the memory unit. After the computation completes, the traceback unit will go back to the previous memory path to read and decode the minimum path metrics that have been stored by ACS unit. This thesis also proposes to remove the add unit in the ACS and traceback unit in the PMU and

replaces it with decoded unit by decoding the code values directly from ACS unit. Moreover, the new algorithm by reducing the complexity of the traditional Viterbi without compromising the performance of the STTC Viterbi decoder has been proposed. Consequently, the number of logic gates and the total power consumption of the STTC Viterbi decoder can be reduced by using the new algorithms. The proposed algorithms have been designed and implemented by using MATLAB, Altera Quartus 2 and Altera MAX V CPLD board. Hence, all results are shown through bit error rate, device utilization, and functional simulation to show the functionality of the hardware design and total power consumption. Results show that more than 43% of the power consumption has been reduced compared to the previous STTC Viterbi decoder designs and achieved 50 MHz clock for 4-PSK modulations.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PEMBANGUNAN PENYAHKOD VITERBI BERKUASA RENDAH PADA PLATFOM PERANTI LOGIK YANG BOLEH DIPROGRAM SEMULA

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"Space Time Trellis Code" (STTC) dan gabungan algoritma Viterbi dikenali untuk menawarkan sistem pembetulan ralat teguh ke hadapan, yang telah digunakan secara meluas dalam sistem komunikasi digital bergangguan seperti komunikasi tanpa wayar. Sebuah penyahkod Viterbi tradisional mengandungi tiga unit utama iaitu Cabang Pengiraan Metrik, Tambah Beza Pilih dan Jalan Pengemaskinian metrik. Gabungan ini akan menyebabkan penyahkod Viterbi mengalami kerumitan dalam proses rekabentuk dan pembangunan. Ia juga akan meningkatkan penggunaan kuasa sistem dan mengurangkan hayat bateri untuk kegunaan peranti mudah alih. Objektif kajian ini adalah untuk menganalisis penggunaan kuasa tinggi oleh penyahkod STTC Viterbi, untuk mereka bentuk model kerumitan yang rendah untuk unit Tambah Beza Pilih dan Jalan Pengemaskinian metrik yang digunakan oleh penyahkod Viterbi dan merekabentuk 0.18µm penyahkod Viterbi yang berkuasa rendah untuk kegunaan STTC. Sebahagian penyahkod menggunakan kaedah maksimum urutan kemungkinan anggaran di dalam rekabentuk penyahkod Viterbi. Ia digunakan untuk mencari kebarangkalian tertinggi dalam memilih nilai terdekat diantara semua jujukan bit yang telah dihantar dengan urutan yang betul. Berdasarkan kajian sebelum ini, diantara ketiga-tiga unit, unit Tambah Beza Pilih dan Jalan Pengemaskinian metrik meggunakan sebahagian besar daripada kuasa dekoder. Tesis ini mencadangkan dua kaedah untuk mengurangkan penggunaan tenaga di dalam penyahkod Viterbi dengan meningkatkan teknik pemprosessan pada unit Tambah Beza Pilih dan unit Jalan Pengemaskinian metrik. Bagi unit Tambah Beza Pilih, kaedah tradisional algoritma Viterbi adalah berfungsi untuk menambah metrik cawangan sebelumnya dengan metrik jalan semasa, membandingkan cawangan baru metrik dan memiilih metrik cawangan yang paling minimum. Kajian ini juga mencadangkan untuk menghapuskan fungsi Tambah dalam algoritma Viterbi ini dengan membandingkan nilai minimum metrik cawangan dari empat keadaan metrik cawangan, memiilih nilai minimum dan mengekod jalan metrik yang minimum.

Bagi unit jalan Pengemaskinian metrik, kaedah tradisional algoritma Viterbi adalah untuk menyimpan nilai minimum yang dipilih oleh jalan metrik pada unit ingatan dan selepas pengiraan selesai, unit traceback akan dapat kembali ke jalan memori sebelumnya untuk membaca dan menyahkod metrik laluan minimum yang disimpan oleh Tambah Beza Pilih. Kajian ini mencadangkan untuk menghapuskan unit add di dalam unit Tambah Beza Pilih dan unit jalan Pengemaskinian metrik di dalam unit pengekod jalan metrik serta menggantikannya dengan unit yang telah dinyahkod oleh penyahkod nilai daripada Tambah Beza Pilih. Kajian ini juga mencadangkan agar algoritma baru yang telah direkabentuk dengan mengurangkan kerumitan Viterbi tradisional tanpa kompromi dalam melaksanakan rekabentuk penyahkod STTC Viterbi. Dengan algoritma baru yang telah direkabentuk, bilangan pintu logik dan penggunaan kuasa dekoder STTC Viterbi dapat dikurangkan. Algoritma yang dicadangkan telah direka dan dibangunkan dengan menggunakan perisian MATLAB, Altera Quartus 2 dan perkakasan Altera MAX V CPLD. Keputusan yang didapati menunjukkan dengan menggunakan kaedah pengiraan kadar kesilapan, pengeluaran penggunaan peranti, simulasi berfungsi untuk menunjukkan fungsi reka bentuk perkakasan dan jumlah penggunaan kuasa. Keputusan menunjukkan bahawa lebih daripada 43% daripada penggunaan kuasa telah dikurangkan berbanding dengan rekabentuk dekoder STTC Viterbi sebelum ini dan rekabentuk penyahkod mencapai frekuensi 50 MHz untuk modulasi 4-PSK.

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I certify that a Thesis Examination Committee has met on 23 March 2018 to conduct the final examination of Mohd Azlan bin Abu on his thesis entitled "Development of Low Power Viterbi Decoder on Complex Programmable Logic Device Platform" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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LIST OF ABBREVIATIONS

ACS	Add Compare Select
ACSout	ACS Output
Add	Addition
ASIC	Application-Specific Integrated Circuit
ASSP	Application-Specific Standard Product
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BM	Branch Metric
BMC	Branch Metric Calculator
clk	Flip Flop Clock Input
CLRN	FF Clear Input (Active High)
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
CSA	Compare Select Add
Ct	Output Bits
D	Data Input From Logic
dB	Decibel
EDA	Electronic Design Automation
EEPROM	Electrical Erasable Programmable Read-Only Memory
ENA	Enable
FPGA	Field Programmable Gate Array
FSG	Faded Symbol Generator
HDL	Hardware Description Language
HSDPA+	High Speed Downlink Packet Access

IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISP	In System Programmability
JTAG	Joint Test Action Group
LTE	Long-Term Evolution
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor Transistor Logic
MHz	MegaHertz
MIMO	Multiple-Input Multiple-Output
MISO	Multiple-Input Single-Output
Mux	Multiplexer
mW	Mili Watt
NMOS	Negative-Channel Metal-Oxide Semiconductor
NRx	Number of Receive Antenna
NTx	Number of Transmit Antenna
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PM	Path Metric
PMOS	Positive- Channel Metal-Oxide Semiconductor
PMU	Path Metric Updater
PRN	Preset Input (Active High)
PSK	Phase-Shift Keying
Q	Output of The Flip-Flop

QPSK	Quadrature Phase Shift Keying
reg	Register
res	Reset
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTL	Register Transfer Level
SIMO	Single-Input Multiple-Output
SM	State Metric
SNR	Signal-To-Noise Ratio
STBC	Space-Time Block Code
STC	Space-Time Code
STTC	Space Time Trellis Code
VCD	Value Change Dump
VHDL	VHSIC Hardware Description Language
VLSI	Very-Large -Scale Integration
Wi-Fi	Wireless Fidelity
WiMAX	Worldwidde Interoperability For Microwave Access
Xt1	Input Bit 1
Xt2	Input Bit 2
3G	Third Generation of Mobile Phone Standards
4G	Fourth Generation of Mobile Phone Standards

CHAPTER 1

INTRODUCTION

1.1 Introduction

The importance of having fast and reliable digital communication network systems has been recognised as one of the necessary facilities in today's life style. Wireless communication network as part of digital communication network is one of few primary medium for information to be easily and quickly disseminated nowadays. The demand for its services is recorded to grow at an accelerated rate over the years (Mallinson, 2015; Thakker, Sarkani, & Mazzuchi, 2012). This high demand for the services has in fact led to a substantial investment in this field that is specifically evident through extensive advancements on wireless communication network.

Digital communication systems have become an essential part of various types of wireless communication devices that allow users to communicate even from a very remote area. Common examples of devices include cell phones, cordless phones, GPS, Wi-Fi, satellite television and computer parts without wires (Joonsuk Kim & Lee, 2015). However, most telecommunication companies have found that the capacity to request a wireless technology is increasing and the cost that is required to install wired technologies such as fiber optics is increasing, especially in areas that are difficult to be reached by wireless technologies (Jens Wiggenbrock ; Kay Smarsly, 2016; Networks et al., 2016).

In order to enable the delivery of the better contents to the users, wireless link capacities must be upgraded. Increasing the capacities can be made by increasing power level of the transmitters or through diversity techniques (Eva Rajo-Iglesias, 2013). Two challenges to increase the level of bandwidth and an existing power are limitation in spectrum and control by authorities (Federal Communications Commission, 2014). These reasons make it difficult or expensive to increase the level of bandwidth and the transmitter existing power. To increase the capacities of the wireless link without increasing the power level, the method of multiplication capacities with the wireless links by using multiple transmitter and receiver antennas for multipath propagation in a wireless communication system through MIMO techniques is explored. MIMO has become an important element in the international wireless communication system standards, such as IEEE 802.11n (Wi-Fi), IEEE 802.11ac (Wi-Fi), HSPA+ (3G), WiMAX (4G), and Long Term Evolution (LTE) (Ayyash et al., 2016; Castaneda, Silva, Gameiro, & Kountouris, 2016; Heath, Gonzalez-Prelcic, Rangan, Roh, & Sayeed, 2016; Zhanji Wu, Gao, & Shi, 2015).

Space-time processing approach is used in communication systems with diversity of the space and time. Spatial diversity is achieved by using various types of antennas either on the sender, recipient, or both parts. This system is known as Multiple Input-Multiple Output (MIMO) for many inputs and many outputs, Single Input-Multiple Output (SIMO) for one input and many outputs and Multiple Input-Single Output (MISO) for many inputs and one output. MIMO can be separated into two parts which are diversity coding technique and spatial multiplexing (Jensen, 2016; Larsson, Edfors, Tufvesson, & Marzetta, 2014).

Diversity coding technique has shown to be an important technique to increase the capacities and enhance the performance of wireless communication systems (Byman, Hulkkonen, Arapoglou, Bertinelli, & De Gaudenzi, 2016). This technique has few versions of the same signals at the receiver to be processed and combined together, either over multiple antennas or called as spatial diversity technique, repeated delivery or called as time diversity technique, and transmitted at different frequencies or called as frequency diversity technique (Larsson et al., 2014). The spatial diversity technique is attractive because it does not expand the bandwidth but the limited numbers of communication spectrum can be shared (Tran & Kong, 2014).

Diversity coding technique is able to improve the accuracy of data transmission for wireless communication systems. This method uses various transmit antennas, which are known as transmit diversity (Di Renzo & Haas, 2013). Transmit diversity technique is a communication system that uses signals from two or more inputs that are not dependent and may change in the characteristics of the transmission at a fast rate. This technique can help to overcome the effects of fading and interference which are major factors of signal losses (Rajashekar, Hari, & Hanzo, 2015). For transmission diversity technique, an additional antenna may be expensive or not practical in a remote area. By using transmit diversity technique, multiple transmit antenna will be transmitted the delayed signal to create a frequency selective fading which will be equalized at the received antenna to produce diversity gain (Di Renzo & Haas, 2013). By using diversity at transmitter and receiver antenna, the received signal depends on the effects of signal fading and signal interference at the receiver (Rajashekar et al., 2015).

To reduce signal integrity degradation that results from multipath fading, the receive diversity technique should be included in RF subsystem of the mobile devices. The diversity technique can reduce the effects of fading by allowing recipients to receive RF signals simultaneously from two different antennas. This method is also used to maximize the quality of the received signals. Receive diversity generates less fading effect on received signals from two antennas. It allows decoders in the baseband processor to perform better operation (Rajashekar et al., 2015). Received diversity also reduces the power requirements at the base station as less power needs to be transmitted to maintain high-quality relation between a base station and mobile phones. By using the diversity in receiver parts, the mobile devices can receive and

process two signals and reduce the impact of a base station for transmitting more power to be dealing with the problem of poor signal quality (C. C. Lu & Wang, 2012).

Diversity coding can be implemented by Space-time coding (STC). STC depends on the delivery of multiple, redundant duplicate of information flows into a recipient in the belief that at least some of that information may be survived on the paths between transmitter and receiver in a state that to be good enough for allowing a trustworthy decoding (Tarokh, Seshadri, & Calderbank, 1998).

Space-time code can be separated into two main parts which are Space time block code (STBC) and Space Time Trellis Code (STTC) (Tarokh et al., 1998). STBC transmits data by using a block of information at a one time. STBC provides diversity gain, but does not provide coding gain (Tarokh, Jafarkhani, & Calderbank, 1999). STTC on the other hand transmits signals by using multiple antennas and multiple time slots. It provides diversity gain, coding gain and better bit error rate (BER) performance (Beygi, Kafashan, Bahrami, Le-Ngoc, & Maleki, 2013).

STTC was discovered by Vahid Tarokh et al. in 1998. STTC distributes the trellis code over multiple time-slots and multiple antennas. STTC encoder generates a parity check code that is sent with an original information. By doing this technique, the coding gain will be obtained (Tarokh et al., 1998). In fact, STTC technique is better than STBC technique to combat severe deterioration in the MIMO channel due to ability of STTC to provide coding gain as contrast to STBC technique (Deergha Rao, 2015; Sandhu, Heath, & Paulraj, 2001). However, STTC decoder that uses the Viterbi algorithm as the decoding method requires larger and more complex decoding technique compared to STBC decoder that uses direct processing especially for wireless applications (Yoo, Jung, Kim, & Lee, 2012).

A Viterbi algorithm was presented in 1967 by Andrew Viterbi. This algorithm acts as a decoding algorithm for convolutional codes in noisy digital communication medium (Viterbi, 1967). In addition, the Viterbi algorithm was used with the combination of STTC to decode a bit stream data that was encoded by using a Space Time Trellis Code (Hong-Du Chen, 2010). Currently, the combinations of the STTC and the Viterbi decoding algorithm are widely used in multicarrier delay diversity modulation systems such as mobile devices, digital radio communication and satellite communication (M.G. El-Mashed ; Sayed El-Rabaie, 2014).

1.2 Problem Statements

The designs and applications of mobile devices are getting more compact and complex (Gao, 2016; Ribeiro, 2013). As a consequence of this, power consumption consume by mobile devices increases and it also causes more battery capacity in order for mobile devices to support the advanced and complex mobile applications such as video streaming, high speed wireless networks and real time cloud computing (Dorairangaswamy, 2016; Queen Kaur Gill ; Kiranbir Kaur, 2016).

The effects of high power consumption for various advanced applications operated in mobile devices are major concerns in the process of designing a Viterbi decoder (He, Liu, Wang, Huang, & Zhang, 2012; Nakashima, 2016; Yoo et al., 2012). Lower power consumption and simpler algorithm complexity requirements have indeed encouraged many researchers to propose many power reduction techniques in the designs of Viterbi decoders (Nakashima, 2016; Putra & Adiono, 2014; Singh & Vishvakarma, 2013).

The combination of STTC and Viterbi decoder has been widely used in designing the MIMO system (M.G. El-Mashed ; Sayed El-Rabaie, 2014; Nakashima, 2016; Putra & Adiono, 2014) . However, despite its ability to provide coding gain and diversity gain, its decoder complexity makes it less favorable to be used in CMOS technology due to high power consumption. This as a result will reduce the battery life of mobile devices (Sugur, Siddamal, & Vemala, 2014; Wang, Zhang, & Chen, 2012).

The Viterbi decoder consists of three parts which are BMC, ACS and PMU. BMC generates branch metric by calculating the distance between transmitting symbols and receiving symbols. ACS unit accumulates branch metrics as a state metric and later compares and selects the minimum state metrics (Viterbi, 1967). Previous findings have shown that ACS unit uses almost 75% power consumption from the total Viterbi decoder power (Guan, Zhou, Wang, Yang, & Zhu, 2009). By transforming Add Compare Select (ACS) module to Compare Select Add (CSA) module, it can reduce nearly 10% power consumption compared to conventional ACS designs (Bhowal, 2013). Finally, PMU unit functions to store the survivor path and do the traceback process for the survived path that extracts the decoded data. Larger memory units are required for storing the path metric and traceback unit of the survivor path. This causes PMU to require a lot of power. They also try to reduce memory access operations of survivor management architecture by up to 30% of the total power consumption (Fu, Li, & Ai, 2013).

Consequently, the Viterbi Algorithm is the best decoding method for designing the decoder for Space Time Trellis code but further improvement in reducing the power consumption needs to be done to increase the battery life for mobile devices.

1.3 Research Objectives

The aim of this project is to develop a new design of Viterbi decoder that can reduce the computation complexity and power consumption for Space Time Trellis Code. Thus the objectives of this thesis include:

1. To design the STTC Viterbi decoder algorithm on MATLAB and Altera Quartus 2.
2. To design the low power Viterbi Decoder by using low complexity model of the ACS and PMU on CPLD device.
3. To design the Verilog code for enhanced STTC Viterbi decoder on Altera Quartus 2 software.
4. To evaluate the low power CPLD for STTC Viterbi decoder in terms of power consumption.
5. To analyse the performance of the BER against SNR for low complexity model of the STTC Viterbi decoder.

1.4 Scope of the Study

This work begins with the selection of the architecture of MIMO system which uses two transmit antennas and two receive antennas. Current studies that indicate the latest mobile phone design employs two received antennas justifies the selection of this architecture (Chattha, Nasir, Abbasi, Huang, & Alja'Afreh, 2013; Ren, 2013).

For the modulation technique selection, this system is designed by using the 4-PSK or QPSK modulation technique. In addition, the QPSK modulation technique is selected because it follows the current modulation scheme standards such as GSM, CDMA, LTE, Wi-Fi, WLAN and WiMAX applications that have been used by modern mobile devices (Mondal, Sardar, & Ananda Babu, 2016).

For the mathematical and algorithm design, Matlab software was used to verify the enhanced STTC Viterbi decoder algorithm in terms of BER by using Monte Carlo Simulation. Figure 1 shows the STTC MIMO system that was designed in the Matlab software which consists of STTC encoder as the transmitter, two transmit antennas, Radio Channel (H) as the path effects with AWGN fading channel was chosen as the noise model, two received antennas and STTC Viterbi decoder that contains of BMC, ACS and PMU as the post parts (Tarokh et al., 1998).

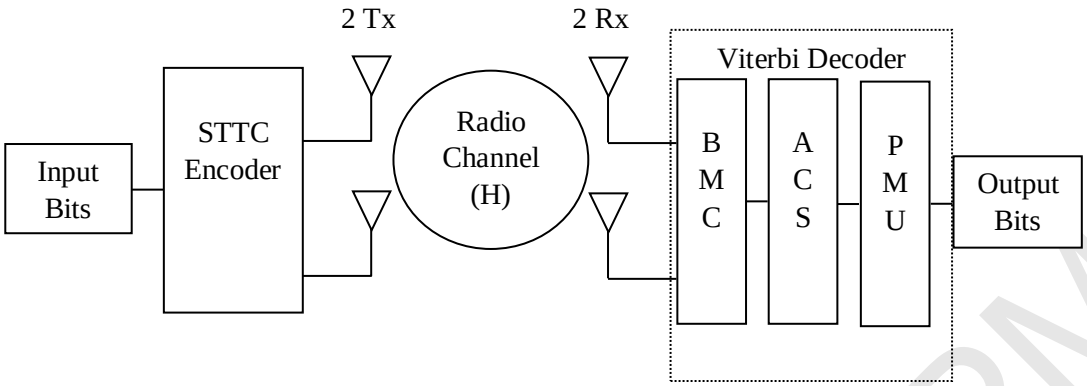

Figure 1.1 : STTC MIMO System
(Tarokh et al., 1998)

For the reconfigurable designs, the STTC Viterbi decoder was designed by using Verilog HDL and implemented in the Max V CPLD. The design focused on the post parts of the Viterbi decoder which consists of the BMC, ACS and PMU only because these three parts are the main contributor to total power consumption in the Viterbi decoder architectures (Hong-Du Chen, 2010). The input signals for the reconfigurable designs were generated by using the functional input generator in the Altera Quartus 2 software.

1.5 Contributions

Resulting from the stated objectives, the contributions of this study can be seen in the following:

1. To propose the low complexity ACS and PMU algorithm for the STTC Viterbi Decoder.
2. To propose the new Verilog code for the enhanced STTC Viterbi decoder.
3. To propose low complexity RTL model for STTC Viterbi decoder.
4. To propose low power STTC Viterbi Decoder by using CPLD.
5. To propose to improve timing performance for the enhanced STTC Viterbi decoder.

1.6 Thesis Outlines

The structure of this thesis reflects the process of designing and developing the low power Space Time Trellis Code Viterbi Decoder by using Complex Programmable Logic Device (CPLD). Thus, this thesis is organized as the following:

Chapter one introduces digital communication in MIMO, STTC and Viterbi decoder. Problems caused by Viterbi decoder are described in the problem statements. This leads to research objectives which have been described in section 1.3. The chapter also includes information on the scope of the thesis and this is followed by section that outlines the study's contributions. Chapter 1 concludes with information on how the thesis is organized.

Chapter two describes the MIMO system, which includes STTC encoder and decoder architecture. Further description of the CMOS circuit power consumption is also described in this chapter. Literatures on Verilog HDL, Altera Quartus 2 software and low power reconfigurable devices are reviewed at the end of this chapter.

Chapter three describes the algorithm for designing the existing STTC Viterbi decoder such as BMC, ACS and PMU. The design flow and power consumption measurement method are also explained in this chapter. Next, the enhancement techniques in designing the STTC Viterbi decoder in the ACS and the PMU parts are described. The final section describes the experimental methods for the enhanced STTC Viterbi decoder.

Chapter four presents the results for the performance of the QPSK modulation by using MATLAB software. The Register Transfer Level Diagram for the existing and enhanced STTC Viterbi algorithm are also shown in this chapter. The functional test and power consumption for existing and the enhanced STTC Viterbi decoder concludes the chapter.

Chapter five draws the conclusions for the thesis which basically summarises the present literature reviews, methodology for existing and enhanced STTC Viterbi decoder and results of the research. Finally, recommendations for future works are presented in this chapter.

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