



UNIVERSITI PUTRA MALAYSIA

***DEVELOPMENT OF LOW POWER VITERBI DECODER ON COMPLEX
PROGRAMMABLE LOGIC DEVICE PLATFORM***

MOHD AZLAN BIN ABU

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PROGRAMMABLE LOGIC DEVICE PLATFORM**

By

MOHD AZLAN BIN ABU

**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia,
in Fulfilment of the Requirements for the Degree of Doctor of Philosophy**

March 2018

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Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Doctor of Philosophy

DEVELOPMENT OF LOW POWER VITERBI DECODER ON COMPLEX PROGRAMMABLE LOGIC DEVICE PLATFORM

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March 2018

Chairman : Associate Professor Noor Izzri Abdul Wahab, PhD, PEng, CEng
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Space Time Trellis Code (STTC) and Viterbi algorithm combinations are known to offer a robust forward error correction system. This especially has been used in a noisy digital communication system such as wireless communication. A traditional Viterbi decoder would contain three main units; Branch Metric Computation Unit (BMC), Add Compare Select Unit (ACS) and path metric updater (PMU). This combination of STTC and Viterbi algorithm however will cause a complexity in STTC decoder and increase power consumption of the system in addition to reducing battery life of portable devices. The objectives of this study are to analyse high power consumption in the STTC Viterbi decoder, design low complexity model of the ACS and the PMU for STTC Viterbi decoder and develop low power 0.18 μ m CMOS Viterbi decoder for STTC. For the decoder, maximum likelihood sequence estimation (MLSE) method has been used in the proposed Viterbi decoder in order to find the highest probability that is selected from all possible transmitted bit sequences which are nearest to the received sequences. ACS and PMU have been reported in previous findings to consume most power of decoder. This thesis thus proposes suitable methods to reduce power consumption in Viterbi decoder by enhancing the ACS and PMU module. For ACS, the traditional method of Viterbi algorithm is to add the previous state metric with the current branch metric, compare the new branch metric and select the minimum branch metric. This thesis however proposes to remove the “Add” function in this Viterbi algorithm by comparing the minimum value of branch metric from the four states of branch metrics, selecting the minimum values and encoding the minimum branch metrics. For the path metric updater unit (PMU), the traditional method of Viterbi algorithm is to store the selected minimum value of branch metric in the memory unit. After the computation completes, the traceback unit will go back to the previous memory path to read and decode the minimum path metrics that have been stored by ACS unit. This thesis also proposes to remove the add unit in the ACS and traceback unit in the PMU and

replaces it with decoded unit by decoding the code values directly from ACS unit. Moreover, the new algorithm by reducing the complexity of the traditional Viterbi without compromising the performance of the STTC Viterbi decoder has been proposed. Consequently, the number of logic gates and the total power consumption of the STTC Viterbi decoder can be reduced by using the new algorithms. The proposed algorithms have been designed and implemented by using MATLAB, Altera Quartus 2 and Altera MAX V CPLD board. Hence, all results are shown through bit error rate, device utilization, and functional simulation to show the functionality of the hardware design and total power consumption. Results show that more than 43% of the power consumption has been reduced compared to the previous STTC Viterbi decoder designs and achieved 50 MHz clock for 4-PSK modulations.



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“Space Time Trellis Code” (STTC) dan gabungan algoritma Viterbi dikenali untuk menawarkan sistem pembetulan ralat teguh ke hadapan, yang telah digunakan secara meluas dalam sistem komunikasi digital bergangguan seperti komunikasi tanpa wayar. Sebuah penyahkod Viterbi tradisional mengandungi tiga unit utama iaitu Cabang Pengiraan Metrik, Tambah Beza Pilih dan Jalan Pengemaskinian metrik. Gabungan ini akan menyebabkan penyahkod Viterbi mengalami kerumitan dalam proses rekabentuk dan pembangunan. Ia juga akan meningkatkan penggunaan kuasa sistem dan mengurangkan hayat bateri untuk kegunaan peranti mudah alih. Objektif kajian ini adalah untuk menganalisis penggunaan kuasa tinggi oleh penyahkod STTC Viterbi, untuk mereka bentuk model kerumitan yang rendah untuk unit Tambah Beza Pilih dan Jalan Pengemaskinian metrik yang digunakan oleh penyahkod Viterbi dan merekabentuk 0.18 μ m penyahkod Viterbi yang berkuasa rendah untuk kegunaan STTC. Sebahagian penyahkod menggunakan kaedah maksimum urutan kemungkinan anggaran di dalam rekabentuk penyahkod Viterbi. Ia digunakan untuk mencari kebarangkalian tertinggi dalam memilih nilai terdekat diantara semua jujukan bit yang telah dihantar dengan urutan yang betul. Berdasarkan kajian sebelum ini, diantara ketiga-tiga unit, unit Tambah Beza Pilih dan Jalan Pengemaskinian metrik menggunakan sebahagian besar daripada kuasa dekod. Tesis ini mencadangkan dua kaedah untuk mengurangkan penggunaan tenaga di dalam penyahkod Viterbi dengan meningkatkan teknik pemprosesan pada unit Tambah Beza Pilih dan unit Jalan Pengemaskinian metrik. Bagi unit Tambah Beza Pilih, kaedah tradisional algoritma Viterbi adalah berfungsi untuk menambah metrik cawangan sebelumnya dengan metrik jalan semasa, membandingkan cawangan baru metrik dan memilih metrik cawangan yang paling minimum. Kajian ini juga mencadangkan untuk menghapuskan fungsi Tambah dalam algoritma Viterbi ini dengan membandingkan nilai minimum metrik cawangan dari empat keadaan metrik cawangan, memilih nilai minimum dan mengekod jalan metrik yang minimum.

Bagi unit jalan Pengemaskinian metrik, kaedah tradisional algoritma Viterbi adalah untuk menyimpan nilai minimum yang dipilih oleh jalan metrik pada unit ingatan dan selepas pengiraan selesai, unit traceback akan dapat kembali ke jalan memori sebelumnya untuk membaca dan menyahkod metrik laluan minimum yang disimpan oleh Tambah Beza Pilih. Kajian ini mencadangkan untuk menghapuskan unit add di dalam unit Tambah Beza Pilih dan unit jalan Pengemaskinian metrik di dalam unit pengekod jalan metrik serta menggantikannya dengan unit yang telah dinyahkod oleh penyahkod nilai daripada Tambah Beza Pilih. Kajian ini juga mencadangkan agar algoritma baru yang telah direkabentuk dengan mengurangkan kerumitan Viterbi tradisional tanpa kompromi dalam melaksanakan rekabentuk penyahkod STTC Viterbi. Dengan algoritma baru yang telah direkabentuk, bilangan pintu logik dan penggunaan kuasa dekoder STTC Viterbi dapat dikurangkan. Algoritma yang dicadangkan telah direka dan dibangunkan dengan menggunakan perisian MATLAB, Altera Quartus 2 dan perkakasan Altera MAX V CPLD. Keputusan yang didapati menunjukkan dengan menggunakan kaedah pengiraan kadar kesilapan, pengeluaran penggunaan peranti, simulasi berfungsi untuk menunjukkan fungsi reka bentuk perkakasan dan jumlah penggunaan kuasa. Keputusan menunjukkan bahawa lebih daripada 43% daripada penggunaan kuasa telah dikurangkan berbanding dengan rekabentuk dekoder STTC Viterbi sebelum ini dan rekabentuk penyahkod mencapai frekuensi 50 MHz untuk modulasi 4-PSK.

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LIST OF ABBREVIATIONS

ACS	Add Compare Select
ACSout	ACS Output
Add	Addition
ASIC	Application-Specific Integrated Circuit
ASSP	Application-Specific Standard Product
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BM	Branch Metric
BMC	Branch Metric Calculator
clk	Flip Flop Clock Input
CLRn	FF Clear Input (Active High)
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
CSA	Compare Select Add
Ct	Output Bits
D	Data Input From Logic
dB	Decibel
EDA	Electronic Design Automation
EEPROM	Electrical Erasable Programmable Read-Only Memory
ENA	Enable
FPGA	Field Programmable Gate Array
FSG	Faded Symbol Generator
HDL	Hardware Description Language
HSDPA+	High Speed Downlink Packet Access

IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISP	In System Programmability
JTAG	Joint Test Action Group
LTE	Long-Term Evolution
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor Transistor Logic
MHz	MegaHertz
MIMO	Multiple-Input Multiple-Output
MISO	Multiple-Input Single-Output
Mux	Multiplexer
mW	Mili Watt
NMOS	Negative-Channel Metal-Oxide Semiconductor
NRx	Number of Receive Antenna
NTx	Number of Transmit Antenna
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PM	Path Metric
PMOS	Positive- Channel Metal-Oxide Semiconductor
PMU	Path Metric Updater
PRN	Preset Input (Active High)
PSK	Phase-Shift Keying
Q	Output of The Flip-Flop

QPSK	Quadrature Phase Shift Keying
reg	Register
res	Reset
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTL	Register Transfer Level
SIMO	Single-Input Multiple-Output
SM	State Metric
SNR	Signal-To-Noise Ratio
STBC	Space-Time Block Code
STC	Space-Time Code
STTC	Space Time Trellis Code
VCD	Value Change Dump
VHDL	VHSIC Hardware Description Language
VLSI	Very-Large -Scale Integration
Wi-Fi	Wireless Fidelity
WiMAX	Worldwide Interoperability For Microwave Access
Xt1	Input Bit 1
Xt2	Input Bit 2
3G	Third Generation of Mobile Phone Standards
4G	Fourth Generation of Mobile Phone Standards

CHAPTER 1

INTRODUCTION

1.1 Introduction

The importance of having fast and reliable digital communication network systems has been recognised as one of the necessary facilities in today's life style. Wireless communication network as part of digital communication network is one of few primary medium for information to be easily and quickly disseminated nowadays. The demand for its services is recorded to grow at an accelerated rate over the years (Mallinson, 2015; Thakker, Sarkani, & Mazzuchi, 2012). This high demand for the services has in fact led to a substantial investment in this field that is specifically evident through extensive advancements on wireless communication network.

Digital communication systems have become an essential part of various types of wireless communication devices that allow users to communicate even from a very remote area. Common examples of devices include cell phones, cordless phones, GPS, Wi-Fi, satellite television and computer parts without wires (Joonsuk Kim & Lee, 2015). However, most telecommunication companies have found that the capacity to request a wireless technology is increasing and the cost that is required to install wired technologies such as fiber optics is increasing, especially in areas that are difficult to be reached by wireless technologies (Jens Wiggerbrock; Kay Smarsly, 2016; Networks et al., 2016).

In order to enable the delivery of the better contents to the users, wireless link capacities must be upgraded. Increasing the capacities can be made by increasing power level of the transmitters or through diversity techniques (Eva Rajo-Iglesias, 2013). Two challenges to increase the level of bandwidth and an existing power are limitation in spectrum and control by authorities (Federal Communications Commission, 2014). These reasons make it difficult or expensive to increase the level of bandwidth and the transmitter existing power. To increase the capacities of the wireless link without increasing the power level, the method of multiplication capacities with the wireless links by using multiple transmitter and receiver antennas for multipath propagation in a wireless communication system through MIMO techniques is explored. MIMO has become an important element in the international wireless communication system standards, such as IEEE 802.11n (Wi-Fi), IEEE 802.11ac (Wi-Fi), HSPA+ (3G), WiMAX (4G), and Long Term Evolution (LTE) (Ayyash et al., 2016; Castaneda, Silva, Gameiro, & Kountouris, 2016; Heath, Gonzalez-Prelcic, Rangan, Roh, & Sayeed, 2016; Zhanji Wu, Gao, & Shi, 2015).

Space-time processing approach is used in communication systems with diversity of the space and time. Spatial diversity is achieved by using various types of antennas either on the sender, recipient, or both parts. This system is known as Multiple Input-Multiple Output (MIMO) for many inputs and many outputs, Single Input-Multiple Output (SIMO) for one input and many outputs and Multiple Input-Single Output (MISO) for many inputs and one output. MIMO can be separated into two parts which are diversity coding technique and spatial multiplexing (Jensen, 2016; Larsson, Edfors, Tufvesson, & Marzetta, 2014).

Diversity coding technique has shown to be an important technique to increase the capacities and enhance the performance of wireless communication systems (Byman, Hulkkonen, Arapoglou, Bertinelli, & De Gaudenzi, 2016). This technique has few versions of the same signals at the receiver to be processed and combined together, either over multiple antennas or called as spatial diversity technique, repeated delivery or called as time diversity technique, and transmitted at different frequencies or called as frequency diversity technique (Larsson et al., 2014). The spatial diversity technique is attractive because it does not expand the bandwidth but the limited numbers of communication spectrum can be shared (Tran & Kong, 2014).

Diversity coding technique is able to improve the accuracy of data transmission for wireless communication systems. This method uses various transmit antennas, which are known as transmit diversity (Di Renzo & Haas, 2013). Transmit diversity technique is a communication system that uses signals from two or more inputs that are not dependent and may change in the characteristics of the transmission at a fast rate. This technique can help to overcome the effects of fading and interference which are major factors of signal losses (Rajashekar, Hari, & Hanzo, 2015). For transmission diversity technique, an additional antenna may be expensive or not practical in a remote area. By using transmit diversity technique, multiple transmit antenna will be transmitted the delayed signal to create a frequency selective fading which will be equalized at the received antenna to produce diversity gain (Di Renzo & Haas, 2013). By using diversity at transmitter and receiver antenna, the received signal depends on the effects of signal fading and signal interference at the receiver (Rajashekar et al., 2015).

To reduce signal integrity degradation that results from multipath fading, the receive diversity technique should be included in RF subsystem of the mobile devices. The diversity technique can reduce the effects of fading by allowing recipients to receive RF signals simultaneously from two different antennas. This method is also used to maximize the quality of the received signals. Receive diversity generates less fading effect on received signals from two antennas. It allows decoders in the baseband processor to perform better operation (Rajashekar et al., 2015). Received diversity also reduces the power requirements at the base station as less power needs to be transmitted to maintain high-quality relation between a base station and mobile phones. By using the diversity in receiver parts, the mobile devices can receive and

process two signals and reduce the impact of a base station for transmitting more power to be dealing with the problem of poor signal quality (C. C. Lu & Wang, 2012).

Diversity coding can be implemented by Space-time coding (STC). STC depends on the delivery of multiple, redundant duplicate of information flows into a recipient in the belief that at least some of that information may be survived on the paths between transmitter and receiver in a state that to be good enough for allowing a trustworthy decoding (Tarokh, Seshadri, & Calderbank, 1998).

Space-time code can be separated into two main parts which are Space time block code (STBC) and Space Time Trellis Code (STTC) (Tarokh et al., 1998). STBC transmits data by using a block of information at a one time. STBC provides diversity gain, but does not provide coding gain (Tarokh, Jafarkhani, & Calderbank, 1999). STTC on the other hand transmits signals by using multiple antennas and multiple time slots. It provides diversity gain, coding gain and better bit error rate (BER) performance (Beygi, Kafashan, Bahrami, Le-Ngoc, & Maleki, 2013).

STTC was discovered by Vahid Tarokh et al. in 1998. STTC distributes the trellis code over multiple time-slots and multiple antennas. STTC encoder generates a parity check code that is sent with an original information. By doing this technique, the coding gain will be obtained (Tarokh et al., 1998). In fact, STTC technique is better than STBC technique to combat severe deterioration in the MIMO channel due to ability of STTC to provide coding gain as contrast to STBC technique (Deergha Rao, 2015; Sandhu, Heath, & Paulraj, 2001). However, STTC decoder that uses the Viterbi algorithm as the decoding method requires larger and more complex decoding technique compared to STBC decoder that uses direct processing especially for wireless applications (Yoo, Jung, Kim, & Lee, 2012).

A Viterbi algorithm was presented in 1967 by Andrew Viterbi. This algorithm acts as a decoding algorithm for convolutional codes in noisy digital communication medium (Viterbi, 1967). In addition, the Viterbi algorithm was used with the combination of STTC to decode a bit stream data that was encoded by using a Space Time Trellis Code (Hong-Du Chen, 2010). Currently, the combinations of the STTC and the Viterbi decoding algorithm are widely used in multicarrier delay diversity modulation systems such as mobile devices, digital radio communication and satellite communication (M.G. El-Mashed ; Sayed El-Rabaie, 2014).

1.2 Problem Statements

The designs and applications of mobile devices are getting more compact and complex (Gao, 2016; Ribeiro, 2013). As a consequence of this, power consumption consume by mobile devices increases and it also causes more battery capacity in order for mobile devices to support the advanced and complex mobile applications such as video streaming, high speed wireless networks and real time cloud computing (Dorairangaswamy, 2016; Queen Kaur Gill ; Kiranbir Kaur, 2016).

The effects of high power consumption for various advanced applications operated in mobile devices are major concerns in the process of designing a Viterbi decoder (He, Liu, Wang, Huang, & Zhang, 2012; Nakashima, 2016; Yoo et al., 2012). Lower power consumption and simpler algorithm complexity requirements have indeed encouraged many researchers to propose many power reduction techniques in the designs of Viterbi decoders (Nakashima, 2016; Putra & Adiono, 2014; Singh & Vishvakarma, 2013).

The combination of STTC and Viterbi decoder has been widely used in designing the MIMO system (M.G. El-Mashed ; Sayed El-Rabaie, 2014; Nakashima, 2016; Putra & Adiono, 2014) . However, despite its ability to provide coding gain and diversity gain, its decoder complexity makes it less favorable to be used in CMOS technology due to high power consumption. This as a result will reduce the battery life of mobile devices (Sugur, Siddamal, & Vemala, 2014; Wang, Zhang, & Chen, 2012).

The Viterbi decoder consists of three parts which are BMC, ACS and PMU. BMC generates branch metric by calculating the distance between transmitting symbols and receiving symbols. ACS unit accumulates branch metrics as a state metric and later compares and selects the minimum state metrics (Viterbi, 1967). Previous findings have shown that ACS unit uses almost 75% power consumption from the total Viterbi decoder power (Guan, Zhou, Wang, Yang, & Zhu, 2009). By transforming Add Compare Select (ACS) module to Compare Select Add (CSA) module, it can reduce nearly 10% power consumption compared to conventional ACS designs (Bhowal, 2013). Finally, PMU unit functions to store the survivor path and do the traceback process for the survived path that extracts the decoded data. Larger memory units are required for storing the path metric and traceback unit of the survivor path. This causes PMU to require a lot of power. They also try to reduce memory access operations of survivor management architecture by up to 30% of the total power consumption (Fu, Li, & Ai, 2013).

Consequently, the Viterbi Algorithm is the best decoding method for designing the decoder for Space Time Trellis code but further improvement in reducing the power consumption needs to be done to increase the battery life for mobile devices.

1.3 Research Objectives

The aim of this project is to develop a new design of Viterbi decoder that can reduce the computation complexity and power consumption for Space Time Trellis Code. Thus the objectives of this thesis include:

1. To design the STTC Viterbi decoder algorithm on MATLAB and Altera Quartus 2.
2. To design the low power Viterbi Decoder by using low complexity model of the ACS and PMU on CPLD device.
3. To design the Verilog code for enhanced STTC Viterbi decoder on Altera Quartus 2 software.
4. To evaluate the low power CPLD for STTC Viterbi decoder in terms of power consumption.
5. To analyse the performance of the BER against SNR for low complexity model of the STTC Viterbi decoder.

1.4 Scope of the Study

This work begins with the selection of the architecture of MIMO system which uses two transmit antennas and two receive antennas. Current studies that indicate the latest mobile phone design employs two received antennas justifies the selection of this architecture (Chattha, Nasir, Abbasi, Huang, & Alja' Afreh, 2013; Ren, 2013).

For the modulation technique selection, this system is designed by using the 4-PSK or QPSK modulation technique. In addition, the QPSK modulation technique is selected because it follows the current modulation scheme standards such as GSM, CDMA, LTE, Wi-Fi, WLAN and WiMAX applications that have been used by modern mobile devices (Mondal, Sardar, & Ananda Babu, 2016).

For the mathematical and algorithm design, Matlab software was used to verify the enhanced STTC Viterbi decoder algorithm in terms of BER by using Monte Carlo Simulation. Figure 1 shows the STTC MIMO system that was designed in the Matlab software which consists of STTC encoder as the transmitter, two transmit antennas, Radio Channel (H) as the path effects with AWGN fading channel was chosen as the noise model, two received antennas and STTC Viterbi decoder that contains of BMC, ACS and PMU as the post parts (Tarokh et al., 1998).

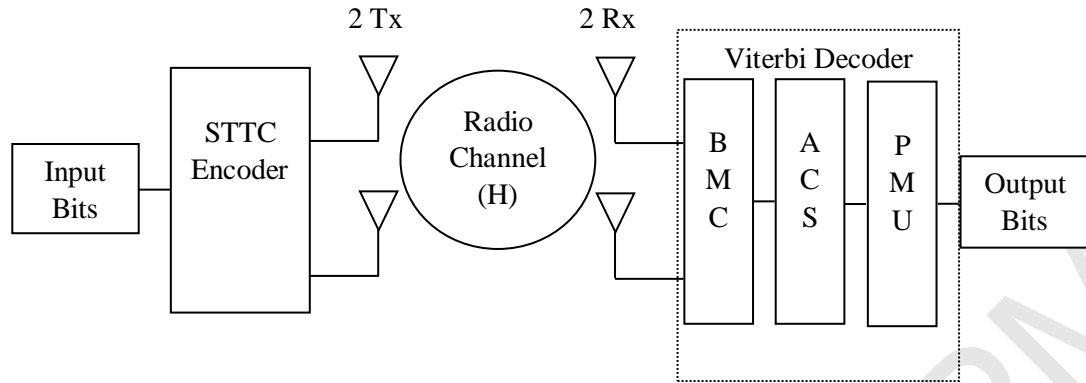


Figure 1.1 : STTC MIMO System
(Tarokh et al., 1998)

For the reconfigurable designs, the STTC Viterbi decoder was designed by using Verilog HDL and implemented in the Max V CPLD. The design focused on the post parts of the Viterbi decoder which consists of the BMC, ACS and PMU only because these three parts are the main contributor to total power consumption in the Viterbi decoder architectures (Hong-Du Chen, 2010). The input signals for the reconfigurable designs were generated by using the functional input generator in the Altera Quartus 2 software.

1.5 Contributions

Resulting from the stated objectives, the contributions of this study can be seen in the following:

1. To propose the low complexity ACS and PMU algorithm for the STTC Viterbi Decoder.
2. To propose the new Verilog code for the enhanced STTC Viterbi decoder.
3. To propose low complexity RTL model for STTC Viterbi decoder.
4. To propose low power STTC Viterbi Decoder by using CPLD.
5. To propose to improve timing performance for the enhanced STTC Viterbi decoder.

1.6 Thesis Outlines

The structure of this thesis reflects the process of designing and developing the low power Space Time Trellis Code Viterbi Decoder by using Complex Programmable Logic Device (CPLD). Thus, this thesis is organized as the following:

Chapter one introduces digital communication in MIMO, STTC and Viterbi decoder. Problems caused by Viterbi decoder are described in the problem statements. This leads to research objectives which have been described in section 1.3. The chapter also includes information on the scope of the thesis and this is followed by section that outlines the study's contributions. Chapter 1 concludes with information on how the thesis is organized.

Chapter two describes the MIMO system, which includes STTC encoder and decoder architecture. Further description of the CMOS circuit power consumption is also described in this chapter. Literatures on Verilog HDL, Altera Quartus 2 software and low power reconfigurable devices are reviewed at the end of this chapter.

Chapter three describes the algorithm for designing the existing STTC Viterbi decoder such as BMC, ACS and PMU. The design flow and power consumption measurement method are also explained in this chapter. Next, the enhancement techniques in designing the STTC Viterbi decoder in the ACS and the PMU parts are described. The final section describes the experimental methods for the enhanced STTC Viterbi decoder.

Chapter four presents the results for the performance of the QPSK modulation by using MATLAB software. The Register Transfer Level Diagram for the existing and enhanced STTC Viterbi algorithm are also shown in this chapter. The functional test and power consumption for existing and the enhanced STTC Viterbi decoder concludes the chapter.

Chapter five draws the conclusions for the thesis which basically summarises the present literature reviews, methodology for existing and enhanced STTC Viterbi decoder and results of the research. Finally, recommendations for future works are presented in this chapter.

REFERENCES

- Ahmed, O. S., Abu-elyazeed, M. F., Abdelhalim, M. B., & Al, E. T. (2013). Logic Picture-Based Dynamic Power Estimation for Unit Gate-Delay Model CMOS Circuits. *Circuits and Systems*, 2013(July), 276–279. Retrieved from <http://linkinghub.elsevier.com/retrieve/pii/S2213020916302208>
- Alsharef, A. A., Mohd Ali, M. A., & Sanusi, H. (2012). Direct digital frequency synthesizer simulation and design by means of quartus-ModelSim. *Journal of Applied Sciences*, 12(20), 2172–2177. <http://doi.org/10.3923/jas.2012.2172.2177>
- Altunbaş, I. (2005). Space-time trellis codes for MSK. *Computers and Electrical Engineering*, 31(4–5), 263–271. <http://doi.org/10.1016/j.compeleceng.2005.05.001>
- Ayyash, M., Elgala, H., Khreishah, A., Jungnickel, V., Little, T., Shao, S., ... Freund, R. (2016). Coexistence of WiFi and LiFi toward 5G: Concepts, opportunities, and challenges. *IEEE Communications Magazine*, 54(2), 64–71. <http://doi.org/10.1109/MCOM.2016.7402263>
- Banerjee, S., & Agrawal, M. (2013). A Simple Analytical Design Approach to Space Time Trellis Codes. *Wireless Personal Communications*, 75(2), 1141–1154. <http://doi.org/10.1007/s11277-013-1412-5>
- Beygi, S., Kafashan, M., Bahrami, H. R., Le-Ngoc, T., & Maleki, M. (2013). Space–Time Trellis Codes for Two-Way Relay MIMO Channels With Single-Antenna Relay Nodes. *IEEE Transactions on Vehicular Technology*, 62(8), 4040–4045.
- Bhowal, S. (2013). Transformation of ACS Module to CSA Module of Low-power Viterbi Decoder for Digital Wireless Communication Applications. In *2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI)* (pp. 266–270). IEEE. <http://doi.org/10.1109/ICACCI.2013.6637182>
- Bobby, N. D., & Srivatsa, S. K. (2011). Implementation of Radix2 ACS in Adaptive Viterbi decoder. *International Conference on Nanoscience, Engineering and Technology (ICONSET)* (2011), 604–606. <http://doi.org/10.1109/ICONSET.2011.6168043>
- Branca Vucetic &, & Jinhong Yuan. (2003). *Space-Time Coding*. John Wiley & Sons Ltd. <http://doi.org/10.1017/CBO9781107415324.004>
- Byman, A., Hulkkonen, A., Arapoglou, P. D., Bertinelli, M., & De Gaudenzi, R. (2016). MIMO for Mobile Satellite Digital Broadcasting: From Theory to Practice. *IEEE Transactions on Vehicular Technology*, 65(7), 4839–4853. <http://doi.org/10.1109/TVT.2015.2462757>

- Castaneda, E., Silva, A., Gameiro, A., & Kountouris, M. (2016). An Overview on Resource Allocation Techniques for Multi-User MIMO Systems. *IEEE Communications Surveys & Tutorials*, 19(c), 1–1. <http://doi.org/10.1109/COMST.2016.2618870>
- Cavallaro, K. C. and J. R. (2001). A Reconfigurable Viterbi Decoder. In *Conference Record of the Thirty-Fifth Asilomar Conference on Signals, Systems and Computers, 2001*. (pp. 66–71). IEEE.
- Cayalag. (2009). STTC decoder. *Cayalag*, 8, 69–72.
- Chattha, H. T., Nasir, M., Abbasi, Q. H., Huang, Y., & Alja' Afreh, S. S. (2013). Compact low-profile dual-port single wideband planar inverted-F MIMO Antenna. *IEEE Antennas and Wireless Propagation Letters*, 12, 1673–1675. <http://doi.org/10.1109/LAWP.2013.2293765>
- Chen, Z., Vucetic, B., Yuan, J., & Lo, K. L. (2002). Space-time Trellis Codes with Two , Three and Four Transmit Antennas in Quasi-Static Flat Fading Channels, 1589–1595.
- Choi, W., Kang, G., & Park, J. (2015). A Refresh-Less eDRAM Macro with Embedded Voltage Reference and Selective Read for an Area and Power Efficient Viterbi Decoder. *IEEE Journal of Solid-State Circuits*, 50(10), 2451–2462. <http://doi.org/10.1109/JSSC.2015.2454241>
- Cholan, K. (2012). Design and implementation of low power high speed viterbi decoder. In *Procedia Engineering* (Vol. 30, pp. 61–68). <http://doi.org/10.1016/j.proeng.2012.01.834>
- Corporation, A. (2007). *Power Optimization in Stratix IV FPGAs* (Vol. 2).
- Corporation, A. (2011). MAX V Device Handbook, 1–166.
- Corporation, A. (2013a). PowerPlay Power Analysis, 1–25.
- Corporation, A. (2013b). Quartus II Handbook Version 13 . 1 Volume 1 : Design and Synthesis, 1, 1–1681.
- Corporation, A. (2013c). *Quartus II Handbook Volume 2: Design Implementation and Optimization* (Vol. 2). Altera Corporation. Retrieved from http://www.altera.com/literature/hb/qts/qts_qii5v2.pdf
- Corporation, A. (2015). *PowerPlay Early Power Estimator User Guide Subscribe Send Feedback*.
- Corporation, I. (2016). *Quartus Prime Standard Edition Handbook Volume 3: Verification* (Vol. 3).
- Deergha Rao, K. (2015). *Channel Coding Techniques for Wireless Communications*. <http://doi.org/10.1007/978-81-322-2292-7>

- Di Renzo, M., & Haas, H. (2013). On transmit diversity for spatial modulation MIMO: Impact of spatial constellation diagram and shaping filters at the transmitter. *IEEE Transactions on Vehicular Technology*, 62(6), 2507–2531. <http://doi.org/10.1109/TVT.2013.2244927>
- Ding, Z., Adachi, F., & Poor, H. V. (2016). The Application of MIMO to Non-Orthogonal Multiple Access. *IEEE Transactions on Wireless Communications*, 15(1), 537–552. <http://doi.org/10.1109/TWC.2015.2475746>
- Dokmanic, I., Parhizkar, R., Ranieri, J., & Vetterli, M. (2015). Euclidean Distance Matrices: Essential theory, algorithms, and applications. *IEEE Signal Processing Magazine*, 32(6), 12–30. <http://doi.org/10.1109/MSP.2015.2398954>
- Dorairangaswamy, K. J. V. ; M. A. (2016). Cloud Framework using Mobile Phone Camera. In *2016 International Conference on Inventive Computation Technologies (ICICT)*. Coimbatore, India: IEEE.
- Eva Rajo-Iglesias. (2013). Printed multi-band MIMO antenna systems and their performance metrics [wireless corner]. *IEEE Antennas and Propagation Magazine*, 55(5), 218–232. <http://doi.org/10.1109/MAP.2013.6735522>
- Fadera, G. N. D., Ignacio, L. R. T., Nastor, M. B. R., Urriza, P. I. M., & Marciano, J. J. S. (2007). FPGA implementation of space-time encoders. In *2007 International Conference on Intelligent and Advanced Systems* (pp. 368–371). Kuala Lumpur: IEEE. <http://doi.org/10.1109/ICIAS.2007.4658410>
- Fadl, O. S., Abu-Elyazeed, M. F., Abdelhalim, M. B., Amer, H. H., & Madian, A. H. (2016). Accurate dynamic power estimation for CMOS combinational logic circuits with real gate delay model. *Journal of Advanced Research*, 7(1), 89–94. <http://doi.org/10.1016/j.jare.2015.02.006>
- Federal Communications Commission. (2014). *FCC-14-30A1*. Washington, D.C. 20554. Retrieved from https://apps.fcc.gov/edocs_public/attachmatch/FCC-14-30A1.docx [
- Fors, K. M., Wiklundh, K. C., & Stenumgaard, P. F. (2013). A simple measurement method to derive the impulsiveness correction factor for communication performance estimation. *IEEE Transactions on Electromagnetic Compatibility*, 55(5), 834–841. <http://doi.org/10.1109/TEMPC.2012.2236090>
- Fu, C., Li, X., & Ai, B. (2013). A Low-Latency and Power-Efficient Viterbi Decoder Based on Dynamic Truncation Length. In *5th IET International Conference on Wireless, Mobile and Multimedia Networks (ICWMMN 2013)* (pp. 367–370). IEEE. <http://doi.org/10.1049/cp.2013.2443>
- Gao, J. H. (2016). Automotive V2X on Phones : Enabling next-generation mobile ITS apps, 858–863.

- García-Zubía, J., Angulo, I., Orduna, P., López-de-Ipina, D., Hernández, U., Rodríguez, L., ... Canivell, V. (2012). WebLab-Deusto-CPLD: A practical experience. *International Journal of Online Engineering*, 8(SPEC. ISSUE), 17–18. <http://doi.org/10.3991/ijoe.v8iS1.1952>
- Gautier, Q., Shearer, A., Matai, J., Richmond, D., Meng, P., & Kastner, R. (2015). Real-time 3D reconstruction for FPGAs: A case study for evaluating the performance, area, and programmability trade-offs of the Altera OpenCL SDK. In *Proceedings of the 2014 International Conference on Field-Programmable Technology, FPT 2014* (pp. 326–329). <http://doi.org/10.1109/FPT.2014.7082810>
- Ghauri, S. A. (2012). Performance of Space Time Trellis Code Using Fading Channel, 523–527.
- Guan, X., Zhou, D., Wang, D., Yang, Y., & Zhu, Z. (2009). A Case Study on Fully Asynchronous ACS Module of Low-power Viterbi Decoder for Digital Wireless Communication Applications. In *2009 International Conference on Computational Intelligence and Natural Computing* (pp. 426–429). IEEE. <http://doi.org/10.1109/CINC.2009.64>
- Habib, I., Paker, Ö., & Sawitzki, S. (2010). Design space exploration of hard-decision viterbi decoding: Algorithm and vlsi implementation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 18(5), 794–807. <http://doi.org/10.1109/TVLSI.2009.2017024>
- Harun, H., Dimyati, K., & Ungku Chulan, U. A. (2013). Optimal generator matrix G. *Aerospace Science and Technology*. <http://doi.org/10.1016/j.ast.2011.10.013>
- He, J., Liu, H., Wang, Z., Huang, X., & Zhang, K. (2012). High-speed low-power viterbi decoder design for TCM decoders. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 20, 755–759. <http://doi.org/10.1109/TVLSI.2011.2111392>
- Heath, R. W., Gonzalez-Prelcic, N., Rangan, S., Roh, W., & Sayeed, A. M. (2016). An Overview of Signal Processing Techniques for Millimeter Wave MIMO Systems. *IEEE Journal of Selected Topics in Signal Processing*, 10(3), 436–453. <http://doi.org/10.1109/JSTSP.2016.2523924>
- Hiller, M., Lima, L. R., & Sigl, G. (2014). Seesaw: An area-optimized FPGA viterbi decoder for PUFs. *Proceedings - 2014 17th Euromicro Conference on Digital System Design, DSD 2014*, 387–393. <http://doi.org/10.1109/DSD.2014.33>
- Hong-Du Chen, & Y.-H. H. S. K. (2010). A Low-Complexity Viterbi Decoder for Space-Time Trellis Codes. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS*, 57(4), 873–885.
- Jain, D., & Sharma, S. (2013). Adaptive Generator Sequence Selection in Multilevel Space-Time Trellis Codes. *Wireless Personal Communications*, 75(4), 1851–

1862. <http://doi.org/10.1007/s11277-013-1440-1>

- Jang, J. E., Park, M., & Kim, J. (2013). An event-driven simulation methodology for integrated switching power supplies in systemverilog. In *Proceedings - Design Automation Conference*. <http://doi.org/10.1145/2463209.2488903>
- Jens Wiggerbrock; Kay Smarsly. (2016). Integrated visualization of installation plans and installation costs of fiber optic networks installation plan with integrated. *Proceeding of Broadband Coverage in Germany; 10. ITG-Symposium*, 26–30.
- Jensen, M. A. (2016). A History of MIMO Wireless Communications. In *2016 IEEE International Symposium on Antennas and Propagation (APSURSI)* (pp. 681–682). <http://doi.org/10.1109/APS.2016.7696049>
- Kahlon, A. S., Szyszkowicz, S. S., Periyalar, S., & Yanikomeroglu, H. (2012). Separating the effect of independent interference sources with rayleigh faded signal link: Outage analysis and applications. *IEEE Wireless Communications Letters*, 1(5), 409–411. <http://doi.org/10.1109/WCL.2012.071612.120392>
- Kavitha, K., & Mangalam, H. (2014). Multilevel Spatial Multiplexing -Space Time Trellis Coded Modulation System for Fast Fading MIMO Channel, 6(1), 273–277.
- Kazaz, T., Kulin, M., & Hadzialic, M. (2013). Design and Implementation of SDR Based QPSK Modulator on FPGA. *IEEE 36th International Convention on Information & Communication Technology Electronics & Microelectronics (MIPRO), 2013*, 513–518.
- Kim, J., & Lee, I. (2015). 802.11 WLAN: History and new enabling MIMO techniques for next generation standards. *IEEE Communications Magazine*. <http://doi.org/10.1109/MCOM.2015.7060495>
- Kim, J., Yoshizawa, S., & Miyanaga, Y. (2012). Variable wordlength soft-decision Viterbi decoder for power-efficient wireless LAN. *Integration, the VLSI Journal*, 45(2), 132–140. <http://doi.org/10.1016/j.vlsi.2011.10.002>
- Larsson, E., Edfors, O., Tufvesson, F., & Marzetta, T. (2014). Massive MIMO for next generation wireless systems. *IEEE Communications Magazine*, 52(2), 186–195. <http://doi.org/10.1109/MCOM.2014.6736761>
- Leventis, P., Vest, B., Hutton, M., & Lewis, D. (2004). MAX II: A low-cost, high-performance LUT-based CPLD. In *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (IEEE Cat. No.04CH37571)* (pp. 443–446). <http://doi.org/10.1109/CICC.2004.1358846>
- Li, Q., Li, G., Lee, W., Lee, M. Il, Mazzaresse, D., Clerckx, B., & Li, Z. (2010). MIMO techniques in WiMAX and LTE: A feature overview. *IEEE Communications Magazine*, 48(5), 86–92.

<http://doi.org/10.1109/MCOM.2010.5458368>

- Li, Y., Vucetic, B., Allan, J. K. A., & Member, S. (2006). On the Performance of Space Time Turbo Trellis Codes with Adaptive Power Allocation, *10*(3), 2–4.
- Liberti, L., Lavor, C., Maculan, N., & Mucherino, A. (2014). Euclidean Distance Geometry and Applications. *SIAM Review*, *56*(1), 3–69. <http://doi.org/10.1137/120875909>
- Lin, C., Shih, Y., Chang, H., & Lee, C. (2005). Design of a power-reduction Viterbi decoder for WLAN applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *52*(6), 1148–1156. <http://doi.org/10.1109/TCSI.2005.849106>
- Lu, C. C., & Wang, J. T. (2012). Throughput-based rate and power control for cognitive radio networks with receive diversity and error control. *IET Communications*, *6*(17), 2848–2854. <http://doi.org/10.1049/iet-com.2011.0528>
- Lu, L., Li, G. Y., Swindlehurst, A. L., Ashikhmin, A., & Zhang, R. (2014). An overview of massive MIMO: Benefits and challenges. *IEEE Journal on Selected Topics in Signal Processing*, *8*(5), 742–758. <http://doi.org/10.1109/JSTSP.2014.2317671>
- M.G. El-Mashed ; Sayed El-Rabaie. (2014). Application of space – time Trellis codes for multicarrier delay diversity modulation systems. *IET Communications*, *8*(17), 3029–3037. <http://doi.org/10.1049/iet-com.2013.0928>
- Mallinson, K. (2015). Smartphone Revolution: Technology patenting and licensing fosters innovation, market entry, and exceptional growth. *IEEE Consumer Electronics Magazine*, *4*(2), 60–66. <http://doi.org/10.1109/MCE.2015.2392954>
- Masud Rana, S., Shamsul Alam, S. M., & Fatema, K. J. (2011). Code construction and performance evaluation of Space Time Trellis Code (STTC) over Rayleigh fading channel. In *14th International Conference on Computer and Information Technology, ICCIT 2011* (pp. 280–285). <http://doi.org/10.1109/ICCITech.2011.6164799>
- Mehzabeen, S. M., & Manju, I. (2013). Efficient Optimization Of FPGA On-Chip Memory For Image Processing Algorithm, (2), 57–61.
- Mishra, D. K., & Saini, L. M. (2016). CPLD based FSK modem for narrowband power line communication. In *Proceeding of IEEE - 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics, IEEE - AEEICB 2016* (pp. 318–321). <http://doi.org/10.1109/AEEICB.2016.7538300>
- Mondal, S., Sardar, S., & Ananda Babu, K. (2016). QPSK modulation and demodulation implementation on CEVA XC-321 DSP for IEEE 802.11b Wi-Fi phone application. *2016 2nd International Conference on Control, Instrumentation, Energy and Communication, CIEC 2016*, 476–480.

<http://doi.org/10.1109/CIEC.2016.7513757>

- Moslehpour, S., Jenab, K., & Siliveri, E. H. (2013). Design and Implementation of NIOS II System for Audio Application. *International Journal of Engineering and Technology (IACSIT)*, 5(5), 627–634. <http://doi.org/10.7763/IJET.2013.V5.631>
- Myburgh, H. C., & Linde, L. P. (2008). Reduced complexity combined Soft-Decision MLSE equalization and decoding. In *Proceedings of the 2008 Australasian Telecommunication Networks and Applications Conference, ATNAC 2008* (pp. 209–213). <http://doi.org/10.1109/ATNAC.2008.4783324>
- Nakashima, H. K. T. H. T. Y. (2016). ASIC Design of A Low-Complexity K-best Viterbi Decoder for IoT Applications. In *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)* (pp. 5–8). IEEE.
- Nakutis, Ž. (2009). Embedded Systems Power Consumption Measurement Methods Overview, (June), 1–8. Retrieved from https://www.researchgate.net/profile/Zilvinas_Nakutis/publication/266013699_Embedded_Systems_Power_Consumption_Measurement_Methods_Overview/links/54c7ade50cf289f0cecd8cd8.pdf
- Networks, E. O., Furdek, M., Szilard, Z., Zhang, J., Ji, Y., Lee, Y., ... Vilalta, R. (2016). Optical Communications Networks. *IEEE Communications Magazine*, 54(8), 108–109.
- Ni, W., Liu, R. P., Biswas, J., Wang, X., Collings, I. B., & Jha, S. K. (2014). Multiuser MIMO scheduling for mobile video applications. *IEEE Transactions on Wireless Communications*, 13(10), 5382–5395. <http://doi.org/10.1109/TWC.2014.2347973>
- Omura, J. (1969). On the Viterbi decoding algorithm. *IEEE Transactions on Information Theory*, 15(1), 177–179. <http://doi.org/10.1109/TIT.1969.1054239>
- Pang, X., Hong, W., Yang, T., & Li, L. (2014). Design and implementation of an active multibeam antenna system with 64 RF channels and 256 antenna elements for massive MIMO application in 5G wireless communications. *China Communications*, 11(11), 16–23. <http://doi.org/10.1109/CC.2014.7004520>
- Patel, D., Bhatt, J., & Trivedi, S. (2015). Programmable logic controller performance enhancement by field programmable gate array based design. *ISA Transactions*, 54, 156–168. <http://doi.org/10.1016/j.isatra.2014.08.019>
- Pradhan, S., & Kumar, G. N. (2013). Design and Implementation of High Speed Low Power Viterbi Decoder, 8(8), 26–32.
- Putra, R. V. W., & Adiono, T. (2014). A configurable and low complexity hard-decision viterbi decoder in VLSI architecture. *2014 2nd International Conference on Information and Communication Technology, ICoICT 2014*,

182–186. <http://doi.org/10.1109/ICoICT.2014.6914062>

- Qam, M. S. P. S. K. (2013). Reduced-Complexity Approx-Log-MAP and. *IEEE Transactions on Communications*, 61(4), 1415–1425.
- Queen Kaur Gill ; Kiranbir Kaur. (2016). A Computation Offloading Scheme for Performance Enhancement of Smart Mobile Devices for Mobile Cloud Computing. In *International Conference on Next Generation Intelligent Systems (ICNGIS)*. Kottayam, India: IEEE.
- Rajab, H. A. (2013). On the Performance of Space Time Trellis Codes on Slow Fading Channels, (2), 0–2.
- Rajashekar, R., Hari, K. V. S., & Hanzo, L. (2015). Quantifying the transmit diversity order of euclidean distance based antenna selection in spatial modulation. *IEEE Signal Processing Letters*, 22(9), 1434–1437. <http://doi.org/10.1109/LSP.2015.2408574>
- Reddy, K. S., & Tech, M. (2013). An Efficient Low Power Viterbi Decoder Design using T-algorithm, 76(5), 5–10.
- Rejection, N. M. (2015). Power Measurements Techniques For Embedded Systems, (March).
- Ren, Y. J. (2013). Ceramic based small LTE MIMO handset antenna. *IEEE Transactions on Antennas and Propagation*, 61(2), 934–938. <http://doi.org/10.1109/TAP.2012.2231660>
- Ribeiro, M. (2013). 5th Generation Touchscreen Controller for Mobile Phones and Tablets Quick design of derivatives.
- Sandhu, S., Heath, R., & Paulraj, A. (2001). Space-time block codes versus space-time trellis codes. *IEEE International Conference on Communications*, 4, 1–11. <http://doi.org/10.1109/ICC.2001.936837>
- Sarkar, S., & Rahman, M. S. (2012). Bit error rate improvement for QPSK modulation technique in a MIMO rayleigh fading channel by maximum likelihood equalization. In *2012 7th International Conference on Electrical and Computer Engineering, ICECE 2012* (pp. 169–173). <http://doi.org/10.1109/ICECE.2012.6471512>
- Shahabinejad, M., & Talebi, S. (2012). Full-diversity space-time-frequency coding with very low complexity for the ML decoder. *IEEE Communications Letters*, 16(5), 658–661. <http://doi.org/10.1109/LCOMM.2012.031212.112648>
- Shr, K., Chen, H., & Huang, Y. (2010). A Low-Complexity Viterbi Decoder for Space-Time Trellis Codes, 57(4), 873–885.

- Singh, P., & Vishvakarma, S. K. (2013). Rtl level implementation of high speed-low power viterbi encoder & decoder. In *2013 IEEE 3rd International Conference on Information Science and Technology, ICIST 2013* (pp. 345–349). Yangzhou, China: IEEE. <http://doi.org/10.1109/ICIST.2013.6747565>
- Song, B., & Park, H. (2013). A binary space-time code for additional diversity gains. *IEEE Transactions on Wireless Communications*, 12(11), 5780–5787. <http://doi.org/10.1109/TWC.2013.093013.130107>
- Soreng, B. (2013). Efficient Implementation of Convolution Encoder and Viterbi Decoder, 1270–1273. <http://doi.org/10.1109/ICCPCT.2013.6529035>
- Suganya, M. G. S., & Ms, G. (2013). RTL Design and VLSI Implementation of an efficient Convolutional Encoder and Adaptive Viterbi Decoder, 494–498.
- Sugur, N. V., Siddamal, S. V., & Vemala, S. S. (2014). Design and implementation of high throughput and area efficient hard decision viterbi decoder in 65nm technology. *Proceedings of the IEEE International Conference on VLSI Design*, 353–358. <http://doi.org/10.1109/VLSID.2014.67>
- Sun, X., Xu, K., Ma, W., Xu, Y., Xia, X., & Zhang, D. (2016). Multi-Pair Two-Way Massive MIMO AF Full-Duplex Relaying With Imperfect CSI Over Ricean Fading Channels. *IEEE Access*, 4, 4933–4945. <http://doi.org/10.1109/ACCESS.2016.2595590>
- Talebi, M. S. F. G. H. S. (2013). Space – Frequency Codes Based on the Space – Time Codes With Very Low Complexity for the Decoder. *IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY*, 62(9), 4678–4684.
- Tang, L., Zhang, X., Zhu, P., & Wang, X. (2016). Wireless Information and Energy Transfer in Fading Relay Channels. *IEEE Journal on Selected Areas in Communications*, 8716(c), 1–1. <http://doi.org/10.1109/JSAC.2016.2612040>
- Tarokh, V., Jafarkhani, H., & Calderbank, a. R. (1999). Space – Time Block Codes from Orthogonal Designs. *IEEE Transactions on Information Theory*, 45(5), 1456–1467. <http://doi.org/10.1109/18.771146>
- Tarokh, V., Seshadri, N., & Calderbank, A. R. (1998). Space-time codes for high data rate wireless communication: Performance criterion and code construction. *IEEE Transactions on Information Theory*, 44(2), 744–765. <http://doi.org/10.1109/18.661517>
- Thakker, R., Sarkani, S., & Mazzuchi, T. (2012). A system dynamics approach to demand and allocation of wireless spectrum for mobile communication. In *Procedia Computer Science* (Vol. 8, pp. 118–123). <http://doi.org/10.1016/j.procs.2012.01.023>
- Tran, T. T., & Kong, H. Y. (2014). Exploitation of spatial diversity in a novel cooperative spectrum sharing method based on PAM and modified PAM

- modulation. *Journal of Communications and Networks*, 16(3), 280–292. <http://doi.org/10.1109/JCN.2014.000048>
- Tuninetti, D. (2014). On the capacity of the AWGN MIMO channel under per-antenna power constraints. In *2014 IEEE International Conference on Communications, ICC 2014* (pp. 2153–2157). <http://doi.org/10.1109/ICC.2014.6883642>
- Vaithiyanathan, D., Nargis, J., & Seshasayanan, R. (2015). High performance ACS for Viterbi decoder using pipeline T-Algorithm. *Alexandria Engineering Journal*, 54(3), 447–455. <http://doi.org/10.1016/j.aej.2015.04.007>
- Verma, P., Sharma, A. K., Pandey, V. S., Noor, A., & Tanwar, A. (2016). Estimation of leakage power and delay in CMOS circuits using parametric variation. *Perspectives in Science*, 8, 760–763. <http://doi.org/10.1016/j.pisc.2016.06.081>
- Veshala, M., Padmaja, T., & Ghanta, K. (2013). FPGA based design and implementation of modified Viterbi decoder for a Wi-Fi receiver. *2013 IEEE Conference on Information and Communication Technologies, ICT 2013*, (Ict), 525–529. <http://doi.org/10.1109/CICT.2013.6558151>
- Vijay Kumar, J., Naga Raju, B., Vasu Babu, M., Sreelekha, K., & Ramanjappa, T. (2016). Implementation of Low Power Pipelined 64-bit RISC Processor with Unbiased FPU on CPLD. *Indian Journal of Science and Technology*, 9(33). <http://doi.org/10.17485/ijst/2016/v9i33/89815>
- Viterbi, A. J. (1967). Error bounds for convolutional codes and an asymptotically optimum decoding algorithm. *IEEE Transactions on Information Theory*, 13(2), 260–269. <http://doi.org/10.1109/TIT.1967.1054010>
- Wang, X., Zhang, Y., & Chen, H. (2012). Design of Viterbi Decoder Based on FPGA. *Physics Procedia*, 24, 1243–1247. <http://doi.org/10.1016/j.phpro.2012.02.186>
- Węgrzyn, M., & Karatkevich, A. (2013). Experimental Comparison of Synthesis Tools Altera Quartus II and Synthesys. *International Journal of Electronics and Telecommunications*, 59(4), 357–362. <http://doi.org/10.2478/eletel-2013-0043>
- Wu, Z., Gao, X., & Shi, Y. (2015). A novel MU-MIMO-OFDM scheme with the RBD precoding for the next generation WLAN. *Proceedings - IEEE Military Communications Conference MILCOM, 2015-Decem*, 565–569. <http://doi.org/10.1109/MILCOM.2015.7357503>
- Wu, Z., Hou, S., & Li, H. (2011). A Light-weighted Viterbi Decoder Implemented by FPGA. *2011 First International Conference on Instrumentation, Measurement, Computer, Communication and Control*, 601–604. <http://doi.org/10.1109/IMCCC.2011.155>

- Yao, J., Yan, H., Das, S., Klemic, J. F., Ellenbogen, J. C., & Lieber, C. M. (2014). Nanowire nanocomputer as a finite-state machine. *Proc Natl Acad Sci U S A*, 111(7), 2431–2435. <http://doi.org/10.1073/pnas.1323818111>
- Ye, J. L., Lin, P., Wang, L. Q., & Zhang, Z. C. (2004). Development of optimized SVPWM algorithm based on CPLD. In *IPEMC 2004: THE 4TH INTERNATIONAL POWER ELECTRONICS AND MOTION CONTROL CONFERENCE, VOLS 1-3, CONFERENCE PROCEEDINGS* (pp. 1603–1606).
- Yoo, W., Jung, Y., Kim, M. Y., & Lee, S. (2012). A pipelined 8-bit soft decision viterbi decoder for IEEE802.11ac WLAN systems. *IEEE Transactions on Consumer Electronics*, 58(4), 1162–1168. <http://doi.org/10.1109/TCE.2012.6414981>
- Yu, Y., & Hill, K. M. (2014). Use of a CPLD in an introductory logic circuits course with software and hardware upgrade. *ASEE Annual Conference and Exposition, Conference Proceedings*, Dassault Systemes (DS); et al.; Kaplan; National I.
- Zeidman, B. B. (2009). Introduction to CPLD and FPGA Design. *Evolution*, 4.
- Zhang, L., Li, Y. X., Li, X. J., & Xu, X. W. (2007). Design and implementation of high speed CCD driving circuit based on CPLD. In *Proceedings of SPIE - The International Society for Optical Engineering* (Vol. 6279 PART). <http://doi.org/10.1117/12.725215>
- Zhang, S., Guo, Q., & Wei, Y. (2015). Performance of cooperative satellite communication based on space-time trellis code. *IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, PIMRC, 2015–Decem*, 1814–1818. <http://doi.org/10.1109/PIMRC.2015.7343593>