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ENHANCED CONTROL ALGORITHMS FOR MULTILEVEL INVERTER-BASED SHUNT ACTIVE POWER FILTER

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By

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Thesis Submitted to the School of Graduates Studies, Universiti Putra Malaysia, in Fullfilment of the Requirement for the Degree of Doctor of Philosophy

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Chair : Mohd Amran Mohd Radzi, PhD
Faculty : Engineering

Nowadays, harmonics mitigations and reactive power compensations are compulsory in power distribution systems due primarily to significant increment of current harmonics and reactive power burden resulted from widespread applications of power electronic devices. Among the existing mitigation solutions, multilevel inverter-based shunt active power filter (SAPF) is potentially to be effective against current harmonics and power factor (PF) degradation, and its mitigation performance is strictly dependent on the quality of its control algorithms.

In this work, three main problems were identified for further investigation. First, dependency on current control algorithm alone is insufficient to solve the severe inherent voltage imbalance problems of multilevel inverters. Second, overall DC-link voltage of SAPF is still regulated using inaccurate yet slow response control algorithms. Third, the existing harmonics extraction algorithms are still exhibiting significant time delay and possessing redundant features.

Therefore, the main aim of this work is to develop new control algorithms which are capable of improving mitigation and dynamic performances of three-level neutral-point diode clamped (NPC) inverter-based SAPF. Specifically, this work focuses on three main control algorithms. Firstly, a simple fuzzy-based dwell time allocation (FDTA) control technique is formulated to enhance the performance of space vector pulse-width modulation (SVPWM) current control algorithm in minimizing inherent voltage imbalance problems of three-level NPC inverter, by suitably adjusting the dwell time of each designated switching state in response to voltage imbalance of DC-link capacitors. Next, a unique inverted error deviation (IED) control technique is incorporated into the main DC-link capacitor voltage regulation algorithm. By utilizing indirect voltage error manipulation approach with reduced computational efforts, the overall DC-link voltage of SAPF is efficiently controlled. Lastly, a new current harmonics extraction algorithm known as simplified synchronous reference

frame (SSRF) algorithm is developed, and with its simplified features, it is able to respond quickly to various system conditions while maintaining high accuracy.

SAPF with all the proposed control algorithms is developed and evaluated in MATLAB-Simulink involving various highly nonlinear rectifier loads. In addition, it is thoroughly evaluated under both steady-state and dynamic-state conditions. Moreover, a laboratory prototype is developed with all the proposed control algorithms downloaded in TMS320F28335 digital signal processor (DSP) board for validation purposes.

From the findings, by incorporating advantages of the proposed FDTA technique, voltages across all the DC-link capacitors are found to be equal, thereby achieving voltage balancing. Without FDTA technique, SVPWM current control algorithm fails to maintain voltage balance of all the DC-link capacitors. Meanwhile, the proposed DC-link capacitor voltage regulation algorithm with IED control technique performs with high accuracy, which is in the range of 99.96 % to 100 %, and fast response time, which is within 0.20 s. Next, by utilizing the proposed SSRF algorithm, SAPF is observed to perform outstandingly with low THD values, which is in the range of 0.96 % to 3.28 % and fast response time, which is within 0.025 s. Finally, mitigation performance of the three-level NPC inverter-based SAPF while using all the proposed control algorithms simultaneously (Set 3) is observed to be the best.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

ALGORITMA KAWALAN TERTINGKAT UNTUK PENAPIS AKTIF KUASA PIRAU BERASASKAN PENYONGSANG BERBILANG ARAS

Oleh

HOON YAP

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Pada masa kini, mitigasi harmonik dan pampasan kuasa reaktif adalah wajib dalam sistem pengagihan kuasa disebabkan terutamanya oleh peningkatan harmonik arus yang ketara dan beban kuasa reaktif yang terhasil daripada penggunaan peranti elektronik kuasa secara meluas. Antara teknik mitigasi yang sedia ada, penapis aktif kuasa pirau (SAPF) berasaskan penyongsang berbilang aras berpotensi untuk berkesan terhadap harmonik arus dan penurunan faktor kuasa (PF), dan prestasi mitigasinya adalah bergantung kuat kepada kualiti algoritma kawalannya.

Dalam kerja ini, tiga masalah utama telah dikenal pasti untuk siasatan lanjut. Pertama, pergantungan kepada algoritma kawalan arus sahaja tidak berupaya untuk menyelesaikan masalah ketidakseimbangan voltan penyongsang berbilang aras yang ketara. Kedua, voltan sambungan DC keseluruhan SAPF masih dikawal menggunakan algoritma kawalan yang tidak tepat lagi perlahan tindak balas. Ketiga, algoritma pengekstrakan harmonik yang sedia ada masih mempamerkan lengah masa yang ketara dan memiliki ciri berlebihan.

Oleh itu, matlamat utama kerja ini adalah untuk membangunkan bagi SAPF berasaskan penyongsang diod terkapit titik neutral (NPC) tiga aras, algoritma kawalan baru yang mampu meningkatkan prestasi mitigasi dan dinamik SAPF. Secara khusus, kerja ini memberi tumpuan kepada tiga algoritma kawalan utama. Pertama, teknik kawalan peruntukan masa inap kabur (FDTA) yang mudah telah dirumus untuk meningkatkan prestasi algoritma kawalan arus pemodulatan lebar denyut ruang vektor (SVPWM) dalam mengurangkan masalah ketidakseimbangan voltan terwujud penyongsang NPC tiga aras, dengan melaraskan masa inap di setiap keadaan pensuisan sebagai tindak balas kepada ketidakseimbangan voltan pemuat sambungan DC. Seterusnya, teknik kawalan sisihan ralat tersongsang (IED) yang unik telah digabungkan dengan algoritma pengaturan voltan pemuat sambungan DC. Dengan menggunakan pendekatan manipulasi ralat voltan tidak langsung dengan penggurangan usaha pengiraan, voltan sambungan DC keseluruhan SAPF dapat

dikawal dengan cekap. Akhir sekali, algoritma pengekstrakan harmonik arus baru yang dikenali sebagai kerangka rujukan segerak dipermudah (SSRF) telah dibina, dan dengan ciri-ciri yang mudah, ia mampu bertindak balas dengan cepat kepada pelbagai keadaan sistem di samping mengekalkan ketepatan yang tinggi.

SAPF dengan semua algoritma kawalan yang dicadangkan telah dibangunkan dan dinilai dalam MATLAB-Simulink yang melibatkan pelbagai beban penerus tak lelurus. Tambahan pula, ia telah dinilai dengan teliti dalam kedua-dua keadaan statik dan dinamik. Selain itu, prototaip makmal juga telah dibina, dengan semua algoritma kawalan yang dicadangkan dimuat turun dalam papan pemproses isyarat digital (DSP) TMS320F28335 untuk pengesahan selanjutnya.

Dari hasil kajian, dengan menggabungkan kelebihan teknik FDTA yang dicadangkan, voltan di semua pemuat sambungan DC didapati sama, sekali gus mencapai keseimbangan voltan. Tanpa teknik FDTA, algoritma kawalan arus SVPWM gagal mengekalkan keseimbangan voltan di semua pemuat sambungan DC. Sementara itu, algoritma pengaturan voltan pemuat sambungan DC dengan teknik kawalan IED yang dicadangkan telah mempamerkan ketepatan yang tinggi, iaitu dalam lingkungan 99.96 % hingga 100 % dan masa tindak balas yang cepat, iaitu dalam lingkungan 0.20 s. Seterusnya, dengan menggunakan algoritma SSRF yang dicadangkan, SAPF didapati beroperasi dengan nilai THD yang rendah, iaitu dalam lingkungan 0.96 % hingga 3.28 % dan masa tindak balas yang cepat, iaitu dalam lingkungan 0.025 s. Akhir sekali, dengan menggunakan semua algoritma kawalan yang dicadangkan secara serentak (Set 3), prestasi mitigasi SAPF berasaskan penyongsang diod terkapit titik neutral (NPC) tiga aras didapati adalah yang terbaik.

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I certify that a Thesis Examination Committee has met on 20 June 2017 to conduct the final examination of Hoon Yap on his thesis entitled "Enhanced Control Algorithms for Multilevel Inverter-Based Shunt Active Power Filter" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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a	Phase A
b	Phase B
c	Phase C
C_{DC}	Effective DC-link Capacitor
C_{DC1}	Upper DC-link Capacitor
C_{DC2}	Lower DC-link Capacitor
$CE(k)$	Change of Voltage Error
d	D Frame Representation
$e_c\,(k)$	Current Error
$E(k)$	Voltage Error
$E_{reg}(k)$	Regulated Voltage Error
I_{DC}	Peak Amplitude of Instantaneous DC-link Charging Current
$i_{1L}\,(k)$	Digital Time-Varying Fundamental Active Current Signal
$i_{1L}\,(t)$	Instantaneous Fundamental Active Current
$i_{DC}(k)$	Digital Time-Varying DC-link Charging Current Signal
$i_{DC}(t)$	Instantaneous DC-link Charging Current
$i_H(k)$	Digital Time-Varying Harmonic Current Signal
$i_H(t)$	Instantaneous Harmonic Current
$i_{inj}(k)$	Digital Time-Varying Injection Current Signal
$i_{inj}(t)$	Instantaneous Injection Current
$i_{inj,ref}(k)$	Digital Reference Injection Current Signal
$i_L(k)$	Digital Time-Varying Load Current Signal
$i_L(t)$	Instantaneous Load Current
$i_S(k)$	Digital Time-Varying Source Current Signal
$i_S(t)$	Instantaneous Source Current
$i_{S,ref}(t)$	Digital Reference Source Current Signal
$IED(k)$	Digital Inverter Error Deviation Signal
f_s	Switching Frequency
k	Numbers of Sampling Data
K_p	Proportional Gain
K_i	Integral Gain
L_f	Filter Inductor
L_l	Line Inductor
M	Modulating Signal
m_a	Modulation Index
q	Q Frame Representation
S	Switching Signal
$sin(\Theta(k))$	Synchronizing Angle
T	Dwell Time
$V_d(k)$	Voltage Deviation
$CV_d(k)$	Change of Voltage Deviation
V_{DC}	Overall DC-link Voltage
$V_{DC}(k)$	Digital Overall DC-link Voltage Signal
$V_{DC}(k-1)$	Previous Digital Overall DC-link Voltage Signal
V_{DC1}	Upper DC-link Capacitor Voltage
$V_{DC1}(k)$	Digital Upper DC-link Capacitor Voltage Signal

V_{DC2}	Lower DC-link Capacitor Voltage
$V_{DC2}(k)$	Digital Lower DC-link Capacitor Voltage Signal
$V_{DC,ref}$	Reference Overall DC-link Voltage
$\vec{V}$	Voltage Vector
$\overrightarrow{V_{ref}}$	Reference Voltage Vector
$v_S(k)$	Digital Time-Varying Source Voltage Signal
$v_S(t)$	Instantaneous Source Voltage
$\theta_{ec}(k)$	Reference Angle of Current Error
$\Delta T(k)$	Incremental Time Interval
Z	Neutral-Point
α	Alpha Domain Representation
β	Beta Domain Representation
0	Zero Domain / Frame Representation

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analogue-to-Digital Converter
AI	Artificial Intelligence
ANN	Artificial Neural Network
APF	Active Power Filter
CCS	Code Composer Studio
CHB	Cascaded H-Bridge
COA	Centre of Area
CSI	Current Source Inverter
DC	Direct Current
DCC	Direct Current Control
DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
DTA	Dwell Time Allocation
EMC	Electromagnetic Compatibility
FC	Flying Capacitor
FDTA	Fuzzy-based Dwell Time Allocation
FFT	Fast Fourier Transform
FLC	Fuzzy Logic Controller
GA	Genetic Algorithm
HPF	High Pass Filter
ICC	Indirect Current Control
IEC	International Electrotechnical Committee
IED	Inverted Error Deviation
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
LPF	Low Pass Filter
NB	Negative Big
NM	Negative Medium
NPC	Neutral-point Diode Clamped
NS	Negative Small
NTV	Nearest Three Vectors
PB	Positive Big
PCC	Point of Common Coupling
PF	Power Factor
PI	Proportional-Integral
PLL	Phase-Locked Loop
PM	Positive Medium
PQ	Instantaneous Power
PS	Positive Small
PWM	Pulse-Width Modulation
rms	Root Mean Square
SAPF	Shunt Active Power Filter
SRF	Synchronous Reference Frame
SSRF	Simplified Synchronous Reference Frame
SVC	Static Var Compensator
SVPWM	Space Vector Pulse-Width Modulation

TDD	Total Demand Distortion
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioner
UPS	Uninterruptible Power Supply
VSI	Voltage Source Inverter
ZCD	Zero-Crossing Detector
ZE	Zero

CHAPTER 1

INTRODUCTION

1.1 Research Background

The rapid advancement in power electronic fields has led to widespread usage of nonlinear loads such as power converters, adjustable speed drives, switched mode power supply, arc furnaces, welding equipment and many others, thereby causing significant power quality problems to the power distribution system. Different classification of power quality problems are identified to be frequency deviation, voltage imbalance, flicker, voltage or current waveform distortion, voltage swells and dips, transient, and harmonics [1-3]. As one of the most hazardous power quality problems, the harmonic currents injected by nonlinear loads causes malfunction of electronic devices, voltage quality degradation, and increased heating and power losses of transformers [4-7]. Moreover, additional reactive power burden caused by the nonlinear loads further degrades the overall system efficiency and worsens power factor (PF) performances. Therefore, it is crucial to minimize the harmonic contents and improve the power factor of power distribution system.

In conjunction with the mitigation efforts, significant harmonic limitation standards such as IEEE standard 519-2014 [8] and IEC 61000-3-2 [9] are established, aimed to limit the negative impacts resulted from nonlinear power system loads. Additionally, a mitigation tool known as power harmonic filter is introduced to reduce harmonic distortion and to improve PF performance. Basically, there are two main power harmonic filters namely passive filter and active power filter, proven to be effective against power quality issues [10-13].

Conventionally, passive filters are fully utilized to deal with harmonic problems. They are recognized as the simplest and most economical mitigation solution. Their configurations typically involve the combination of simple passive elements (resistors, capacitors and inductors) [10, 14]. However, they could be tuned to attenuate selected harmonics present in the line current, thereby limiting their mitigation ability. They are only capable to solve harmonics resulted from specific type of nonlinear loads and cannot work directly with dynamic load conditions which occur regularly in power system. Therefore, it is very difficult for these filters to meet the mitigation requirements for varying harmonics and reactive power.

Owing to the limitations of conventional mitigation methods, a more powerful harmonic mitigation tool known as active power filter (APF) is introduced. Basically, APF is developed based on modern power electronics technology. The modern APF possesses the ability to overcome the weaknesses of conventional passive filters. In contrast to conventional passive filters, the modern APFs are superior in terms of filtering performance, more flexible in dealing with harmonics of various levels, yet physically smaller [15]. A typical APF could eliminate the harmonics present in the

power system by injecting equal harmonics in opposite phase into the power line, thereby improving the power quality of the connected power system. APFs also can be referred as active power quality conditioners, active power line conditioners, and self-commutated static Var compensators (SVCs). In other words, their applications are not limited to harmonic filtering, but are also applicable in harmonic isolation, harmonic damping, harmonic termination, reactive power control for power factor correction and for voltage regulation, load balancing, voltage flicker reduction, and any of their combinations [15].

Various types of APFs have been reported in the literature [15-17] and they are divided into single phase (two-wire) [15] and three-phase (three-wire and four-wire) APFs [17], depending on their applications. Moreover, they are also classified into series [18, 19] and shunt [20-22], depending on their respective circuit configurations. Furthermore, a combination of series and shunt APFs known as unified power-quality conditioner (UPQC) [23-25], and hybrid APF topology [26-28] which utilizes the strength of passive and active filters, are also well investigated serving as another alternative in power quality improvement. Nonetheless, shunt APFs (SAPFs) are the most widely applied topology in current harmonics mitigation, reactive power compensation, and three-phase current balancing.

Previously, most SAPFs utilize standard two-level voltage source inverters (VSIs) in their design [29, 30]. They have been recognized as the best solution to eliminate harmonics in low and medium power systems. They provide simple circuit structure, and thus simpler control strategies are needed. However, they require large rating DC-link capacitor and power semiconductor switching devices which increase the cost and system losses. Recently, multilevel inverters have brought a new dimension to SAPF by providing significant advantages over conventional two-level inverters. They are superior in term of output voltage quality where lower harmonic distortion is achieved through the generation of output with higher voltage levels. Moreover, having multiple levels of output voltages also contribute to lower switching frequency and lower power losses. However, SAPFs based on multilevel inverter are more complicated than two-level inverter due primarily to higher amount of switching devices and DC-link capacitors. Besides, high usage of DC-link capacitors further causes voltage imbalances across the DC-link capacitors. They are recognized as the inherent problems of multilevel inverters which must be overcome to ensure proper function of SAPF. Therefore, a comprehensive control strategy is needed to control the complex switching operation of multilevel inverter, and at the same time, for maintaining the voltage balance of all DC-link capacitors.

Multilevel inverter configurations are mostly considered for high power medium voltage applications due to their unique ability in providing higher output voltage. However, in another point of view, it will be very interesting to apply them in low power and voltage side due to their unique features in reducing voltage stresses across power switching devices which will allow the usages of lower rated devices in their designated applications. In this manner, the economical features of the designed SAPF can be improved. Besides, when it comes to SAPF applications, it is more worthwhile to utilize the advantages of multilevel inverter at low voltage side where

harmonic problems are more severe. In fact, in low voltage applications, multilevel inverters have widely been reported and are proven to exhibit better performance and economical features as compared to two-level inverters [31-33].

In the context of SAPF, there are three most widely reported multilevel inverter configurations. These include neutral-point diode clamped (NPC) [21, 34], cascaded H-bridge (CHB) [20] and flying capacitor (FC) multilevel [35]. Nevertheless, NPC multilevel inverter is the most preferred for SAPF implementation as it provides the best advantages in terms of DC-link capacitor voltage balancing by requiring the least amount of capacitors as compared to the other topologies [36, 37]. Moreover, the multilevel inverters employed for SAPF applications are mostly restricted to three-level inverters due to great difficulties in controlling the higher amount of switching states and more severe voltage imbalances will happen to the capacitors as the number of level increases [20, 21, 34].

The effectiveness of SAPF in power quality mitigation is strictly dependent on how quickly and how accurately its control strategies work. Various control strategies of SAPFs have been discussed in [38-40]. Generally, the control strategies of SAPF consist of three main control algorithms namely harmonics extraction (also known as reference current generation), DC-link capacitor voltage regulation (usually applied in inverter-based SAPF) and current control (also known as switching) algorithms. However, for multilevel inverter-based SAPF, the current control algorithm must be expanded so that it is able to effectively control the higher switching states of multilevel inverter [41]. Moreover, additional control technique must be incorporated into the current control algorithm to minimize its voltage imbalance problems by controlling the charging and discharging of DC-link capacitors [42]. Basically, the techniques used to achieve voltage balancing of DC-link capacitors vary according to the current control algorithm applied. In other words, a complete understanding on the operation of multilevel inverter and SAPF must be acquired so that a good compromise between voltage balancing technique and current control algorithm can be achieved to effectively deal with the voltage imbalance problems.

For three-level NPC inverter-based SAPF, the voltage across the splitting DC-link capacitors must equally be maintained as half of the overall DC-link voltage. Among all the existing current control approaches as reported by Rodriguez, Lai and Peng [36], space vector pulse-width modulation (SVPWM) algorithm is the most attractive choice due to its high flexibility in switching states selection, forming variety of optimal switching sequences to suit different types of inverter topologies.

In the context of SVPWM, unequal operations of small and medium vectors are recognized as the prime causes of neutral-point voltage deviation which leads to imbalance of DC-link capacitor voltage. Conventionally, SVPWM relies solely on symmetrical switching sequence design with equal dwell (conduction) time allocation for N-type and P-type small vectors to achieve natural balancing of DC-link capacitor voltages [43, 44]. However, by depending on fixed dwell time allocation approach cannot completely solve the severe voltage deviation problems

of NPC inverter, especially when it operates as SAPF. Moreover, in practical situation, fixed dwell time allocation approach is incapable of dealing with time-varying systems which may further worsen the voltage deviation, as demonstrated by Bhat et al. [45].

Further improvement which involve rearrangement of switching sequence has been introduced by Abdelkrim et al. [46]. In this technique, redundant small vectors are rearranged to suit different imbalance conditions of DC-link capacitor voltage. However, rearrangement of switching sequences requires large development of complex switching sequences, thereby it is a time consuming method. A better alternative is proposed by Choi and Lee [47], where the dwell time of N-type and P-type small vectors are adjusted accordingly to deal with different voltage imbalance conditions of DC-link capacitors. The dwell time adjustment method is effective against various types of voltage imbalance conditions and does not require any complex switching sequence design. However, it is difficult to precisely determine the amount of time adjustment needed to accurately deal with voltage imbalance problems. In most solutions, the time adjustment value is predicted using complex mathematical analysis, and thus complicates hardware development [42, 47].

Next, in the context of inverter-based SAPF, the overall DC-link voltage must constantly be maintained at a level which is high enough to precisely inject the desired injection current back to the polluted power system. Conventionally, overall DC-link voltage is regulated via direct voltage error manipulation approach where the difference (voltage error) between actual overall DC-link voltage and its desired reference voltage is directly utilized by either proportional-integral (PI) controller [48-50] or fuzzy logic controller (FLC) [51-53], to produce an estimated output which is assumed to be the main control signal for regulating DC-link voltage.

PI technique is more widely used due to its simple implementation features. The overall DC-link voltage can be regulated just by applying a fixed value of proportional gain K_p and integral gain K_i. However, due to the use of fixed gain values, PI technique is unable to work satisfactory under dynamic-state conditions. This greatly affects performance of SAPF in regulating DC-link voltage and mitigating harmonic currents. Moreover, the tuning procedure for the determination of optimal gain values is very time consuming, as reported by Suetake, Silva and Goedtel [54]. Hence, it is not worthwhile to allocate such a long time just to obtain a fixed value of gain.

On the other hand, FLC technique is currently the best method in regulating the overall DC-link voltage. Its control ability far surpasses performance of the PI technique [48, 50, 55]. It is an adaptive mechanism which is able to perform effectively with imprecise inputs, handle nonlinear or time-varying system, and is possible to be designed without knowing the exact mathematical model of the system [52, 56]. However, in the context of overall DC-link voltage regulation, the FLC techniques employed are mostly implemented with high number of fuzzy membership functions and rules, thereby imposing great computational burden to the controller [49, 51, 57].

Furthermore, synchronous reference frame (SRF) algorithm has served the major role in current harmonics extraction and reference current generation due to its superior advantages over the other available algorithms such as simple design and fast computational speed. However, the latest trend in SRF algorithm is still relying on numerical filters especially low pass filter (LPF) to detect the desired fundamental component for reference current generation [58-60]. The dependency on sluggish numerical LPF which suffers from serious time delay has significantly limited the detection performance. For instance, Wang et al. [59] have demonstrated that the existing SRF performs within 0.05 s (2.5 cycles of 50 Hz signal). Moreover, tuning procedure for the determination of cutting frequency value is very time consuming as it is normally realized through tedious heuristic approach. Furthermore, a good compromise between cutting frequency and the order of filter is difficult to be attained but it is required to ensure optimum performance.

Another weakness of existing SRF algorithm is related to the characteristic of its generated reference current. To date, the existing SRF algorithm is still producing a non-sinusoidal reference current through derivation of the extracted harmonic current [58, 61, 62]. As a result, it forces the switching signals meant for controlling the switching activities of SAPF to be generated based on direct current control (DCC) scheme [63-65].

As reported in [17, 65, 66], the switching operation of SAPF produces switching ripples in the source current, which undoubtedly degrades the THD performance of the mitigated source current. However, DCC scheme which operates based on comparison of measured injection current with its non-sinusoidal reference current counterpart does not possess accurate information on the shape of the actual source current. Therefore, even if the source current is polluted by switching ripples, the DCC scheme will not be able to mitigate the ripples due to lack of exact information. Although indirect current control (ICC) scheme which operates based on comparison of actual source current with its sinusoidal reference current counterpart [63-66] has been revealed to overcome the weakness of DCC scheme, there is still no relevant work on SRF algorithm which has been conducted together with ICC scheme. In fact, working principle of the existing SRF algorithm itself limits its application solely to DCC scheme.

1.2 Problem Statement

This work focuses on implementation of current control algorithm with neutral-point voltage deviation control technique (voltage balancing technique), DC-link capacitor voltage regulation and harmonics extraction algorithms, for improving performance of a three-level NPC inverter-based SAPF in maintaining the voltage balance of splitting DC-link capacitors, regulating overall DC-link voltage, generating reference currents and mitigating harmonic currents.

For multilevel inverter applications, it is very crucial to first deal with their inherent voltage imbalance problems. In three-level NPC inverter-based SAPF, voltage

imbalance across its splitting DC-link capacitors is particularly due to unequal operation of its control system, and could be further worsen by fabrication tolerances dissimilar characteristic of its switching devices. Although the existing methods have performed well in minimizing the voltage imbalance issues, they mostly depend on complex mathematical analysis to operate, thereby complicating the control structure.

Besides that, dynamic-state conditions are unavoidable in SAPF operation especially for its DC-link capacitor voltages. The DC-link capacitors may blow if they experience a sudden increase of voltage, and also SAPF may not work properly if its DC-link capacitors experience a sudden drop of voltage. Since the PI and FLC techniques applied in existing DC-link capacitor voltage regulation algorithms are still operated based on direct voltage error manipulation approach where the entire voltage error signal is processed without giving enough attention to voltage deviations (overshoot and undershoot) that occur to the overall DC-link voltage throughout the operation of SAPF, hence they cannot completely eliminate the severe DC-link voltage deviation that occurs during dynamic-state conditions. This leads to high overshoot, undershoot and slow response time during dynamic operation of SAPF.

Furthermore, the existing SRF algorithm which has performed effectively in current harmonics extraction still considered to possess unnecessary features which do not represent the basic requirements of current harmonics extraction. These include the existing of cosine and zero-sequence components which potentially increases computation burden of the algorithm. Moreover, its main weaknesses which include dependency on numerical LPF and ability to generate non-sinusoidal reference current must be improved to further enhance mitigation performance of SAPF.

Apart from the aforementioned problems, to date, research works on multilevel inverter-based SAPF are actually still very limited, and would require further comprehensive evaluation and analysis to verify their effectiveness and feasibility.

1.3 Aim and Objectives

The main aim of this work is to enhance performance of three-phase three-wire three-leg three-level neutral-point diode clamped (NPC) inverter-based shunt active power filter (SAPF) in minimizing line harmonic currents and improving line power factor with new control algorithms. The objectives of this work are;

1. To design and develop for the NPC inverter-based SAPF, a current control algorithm with new neutral-point voltage deviation control technique known as fuzzy-based dwell time allocation (FDTA) technique.
2. To design and develop for the NPC inverter-based SAPF, a new DC-link capacitor voltage regulation algorithm with inverted error deviation (IED) control technique.
3. To design and develop for the NPC inverter-based SAPF, a new current harmonic extraction algorithm which operates with ICC scheme known as simplified synchronous reference frame (SSRF) algorithm.

4. To evaluate overall performance of the NPC inverter-based SAPF with simultaneous implementation of the proposed FDTA, IED and SSRF control algorithms.

Simulation model of NPC inverter-based SAPF is developed and simulated together with the proposed control algorithms under various steady-state and dynamic-state conditions. A hardware prototype of the proposed design is then developed in the laboratory to examine and verify its performance.

1.4 Scope and Limitations of Work

The scope of this work is divided into two sections namely software and hardware sections. In the software section, the work begins with the design of three-phase three-wire three-leg three-level NPC inverter-based SAPF followed by simulation of the proposed design in MATLAB-Simulink software program. Three-phase three-wire system is considered for this work due to wider applications of power electronics devices in three-phase applications which lead to significant spread of current harmonics in three-phase power system, and thus make it compulsory to be mitigated efficiently.

Additionally, in order to further improve mitigation performance of SAPF, multilevel inverter which provides better output quality is employed in this work rather than depending on standard two-level VSI. However, in SAPF's applications, the multilevel inverters employed are mostly restricted to three-level inverters due to complexity of controller design which involves larger number of switching states and greater severity of voltage imbalance to the capacitors as the number of level increases [20, 21, 34]. Meanwhile, the selection of multilevel inverter topology is performed by considering the severity of voltage imbalance problems exhibited by that particular topology. Therefore, NPC multilevel inverter which requires the least amount of DC-link capacitors is employed for this work. As a result, less effort is needed to balance up the voltage across all the DC-link capacitors of NPC multilevel inverter, and thus reduces complexity of the designed controller.

The development of three-phase three-wire three-leg three-level NPC inverter-based SAPF involves the design of three-phase three-wire three-leg three-level NPC inverter-based SAPF circuits together with its controller, which comprises of four main algorithms known as current control algorithm with neutral-point voltage deviation control technique, DC-link capacitor voltage regulation algorithm, current harmonics extraction algorithm and synchronizer algorithm. However, this research work only focuses on three most important algorithms which include current control algorithm with neutral-point voltage deviation control technique, DC-link capacitor voltage regulation algorithm and current harmonics extraction algorithm, for implementing further improvements.

In simulation work, the input source voltage is set to be 400 Vrms (line-to-line). The three-phase three-level NPC inverter-based SAPF and all the control algorithms involved are developed using SimPower System blocks. Three types of highly nonlinear loads, as reported in [6, 67, 68] are applied in this work to test the performance of SAPF under steady-state and dynamic-state conditions. The first nonlinear load is constructed using a three-phase uncontrolled bridge rectifier feeding a 20 Ω resistor and 2200 μF capacitor connected in parallel (capacitive). Meanwhile, the second nonlinear load is developed using similar rectifier feeding a series connected 50 Ω resistor and 50 mH inductor (inductive). The third nonlinear load is developed using similar rectifier feeding a 50 Ω resistor (resistive). Under steady-state condition, THD value and power factor are the main parameters used to evaluate performance of the proposed SAPF. Meanwhile, under dynamic-state condition, the proposed SAPF is evaluated for its dynamic response when encountering sudden nonlinear load change. For this analysis, two dynamic-state conditions are created by changing the nonlinear load from capacitive to inductive and inductive to resistive, respectively.

Evaluation under unbalanced and distorted source voltage is out of scope because according to working principle of SAPF, source voltage serves as a reference to ensure proper synchronization between voltage and current so that opposition harmonic mitigating current can accurately be injected back into the power line to mitigate the presence of current harmonics [15, 67, 69]. Therefore, this work only considers balanced three-phase three-wire system with sinusoidal source voltage.

In the hardware section, a laboratory prototype is constructed where the controller and power circuits are assembled to function as a three-phase three-level NPC inverter-based SAPF, similar to the one that is modelled in MATLAB-Simulink. In experimental work, for safety purposes and due to limitation of resources, the input source voltage is set to be 100 Vrms (line-to-line), which is supplied by programmable AC source. Meanwhile, a high performance digital signal processor (DSP) is programmed to perform all the control algorithms of the SAPF. The laboratory prototype is tested under both steady-state and dynamic-state conditions with similar capacitive, inductive and resistive nonlinear loads, as in the simulation work. Similarly, evaluation in terms of THD value, power factor, and dynamic response is conducted. In addition, the results obtained are validated with the simulation work.

1.5 Thesis Layout

This thesis is organized into five chapters. Chapter 1 provides brief introduction on the research work which includes research background, main problems to be solved, aim and objectives, and scope and limitations of the work.

Chapter 2 defines power quality, states distinctive categories of power quality problems, and discusses harmonics as one of the main power quality problems. A survey on harmonics mitigation strategies which include the commonly applied

harmonic standards and harmonics mitigation tools are also provided. Next, comprehensive review on multilevel inverter-based SAPF as the most effective solution to current harmonics is presented, focusing on its principles of operation and control strategies applied. Additionally, comparative study on characteristics, advantages and limitations of three most promising multilevel inverter configurations are provided, serving as a guideline to select the best multilevel inverter for a specific application.

Chapter 3 describes the design and development of three-phase three-wire three-leg three-level NPC inverter-based SAPF, detailing its operating principle and design considerations. Moreover, the newly proposed control algorithms are clearly described. This chapter also provides complete details on simulation model and laboratory setup of the proposed SAPF as well as implementation of the proposed control algorithms in a high performance DSP.

Chapter 4 presents the findings and results obtained in simulation and experimental works. Comparative evaluation is presented, highlighting the improvements achieved by all the proposed control algorithms in comparison to their corresponding existing benchmark algorithms. Moreover, overall improvements achieved by SAPF with simultaneous implementation of all the proposed control algorithms are also presented.

Chapter 5 concludes the work, significant contributions of the work and recommends possible future works.

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