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DESIGN AND IMPLEMENTATION OF LOW COMPLEXITY OFDM MODULATOR FOR BROADBAND WIRELESS DEVICES

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DESIGN AND IMPLEMENTATION OF LOW COMPLEXITY OFDM MODULATOR FOR BROADBAND WIRELESS DEVICES

By

KHALID TAHER MOHAMMED AL-HUSSAINI

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

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DEDICATIONS

قال تعالى

﴿ قَالُوا سُبْحَانَكَ لَا عِلْمَ لَنَا إِلَّا مَا عَلَّمْتَنَا إِنَّكَ أَنْتَ الْعَلِيمُ الْحَكِيمُ ﴾

البقرة (32)

I would like to dedicate this thesis to my beloved motherland
"YEMEN".

&

To the loving memory of my parents,
"May Allah bless them with his supreme benevolence" who is
forever remembered. To my caring, lovely wife, sisters, brothers, and friends, who have
supported me all the
way since the beginning of my study to my dear friends for their moral support,
inspiration and guiding hand on my life in Malaysia.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Doctor of Philosophy

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March 2017

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The modulation technique plays significant role as a component of communication systems. A novel technique known as orthogonal frequency division multiplexing (OFDM), which can be implemented in broadband wireless systems, has been designed and developed to fulfill the requirements of high data rate signals. One of the major drawbacks of OFDM systems is its high crest factor (CF) in the time domain. The large CF causes the transmit power amplifier to enter the non-linear region, distorting the signal and resulting in a significant increase in the bit error rate (BER) at the receiver.

This thesis focuses on the design and implementation of a proposed techniques approach to reduce CF, and the computational complexity of the proposed techniques will increase linearly with the increase of the number of subcarriers. This research presents three novel low complexity techniques for reducing CF in OFDM systems followed by an efficient hardware co-simulation implementation of two of these techniques by using a Xilinx system generator on a field programmable gate array (FPGA).

The first part of this thesis presents a new subblocks interleaving partial transmit sequence (SBI-PTS) technique having low complexity for reducing the CF in OFDM systems followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on a field programmable gate array (FPGA). In this technique, a new subblocks interleaver is proposed. The subblocks interleaver can be applied in the frequency domain before the inverse fast Fourier transforms (IFFT) or in the time domain after (IFFT). Moreover, a new optimization scheme is introduced, in which the number of iterations is made to be equal to the number of subblocks only which results in

reduced processing time and less computation that leads to reduced complexity.

A new low complexity high efficiency hybrid multiplicative-additive CF reduction technique for OFDM systems is presented in the second part of the thesis. This technique consists of two IFFT blocks. First, the output of the two IFFT blocks is partitioned into four subblocks, which are subsequently used to rearrange the subblocks with padding zeros in a specific manner. Then, a new optimization scheme is introduced, in which only a single two-phase sequence and four iterations needs to be applied. Numerical analysis shows that the hybrid proposed technique achieves better CF reduction performance with significantly lower complexity and better bit error rate performance than the existing scrambling (multiplicative) and additive CF techniques. The other salient feature of this scheme is that no side information (SI) is needed which increases transmission efficiency.

The last part of this thesis presents a new low complexity scrambling technique for reducing the CF in OFDM systems followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on a FPGA. In this technique, the output of a single IFFT is duplicated M times and partitioned into M subblocks, which are subsequently interleaved. Then, a new optimization scheme is introduced in which only a single two phase sequence need to be applied. Unlike the C-PTS which needs M- IFFT blocks and 2^{M-1} iterations, the proposed technique requires only a single IFFT block and M iterations. These features significantly reduce processing time and less computation that leads to reduced complexity. Simulation results demonstrate that the new technique can effectively reduce the complexity up to 99.95% compared with the conventional PTS (C-PTS) technique and yields good CF performance.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

REKA BENTUK DAN PELAKSANAAN RENDAH KERUMITAN OFDM MODULATOR UNTUK PERANTI TANPA WAYAR JALUR LEBAR

Oleh

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Teknik modulasi memainkan peranan penting sebagai salah satu komponen sistem komunikasi. Satu teknik baharu yang dikenali sebagai pemultipleksan pembahagian frekuensi ortogonal (OFDM), yang boleh dilaksanakan dalam sistem tanpa wayar jalur lebar, telah direka dan dibangunkan untuk memenuhi keperluan kadar data yang tinggi. Salah satu kelemahan utama sistem OFDM adalah faktor puncak (CF) yang tinggi dalam domain masa. CF yang besar menyebabkan penguat kuasa penghantar untuk memasuki rantau tak linear, mengganggu isyarat dan menyebabkan peningkatan yang ketara dalam kadar ralat bit (BER) pada penerima.

Tesis ini memberi tumpuan kepada reka bentuk dan pelaksanaan pendekatan teknik yang dicadangkan untuk mengurangkan CF, dan kerumitan pengiraan teknik yang dicadangkan akan meningkat secara linear dengan peningkatan bilangan pecahan pembawa. Kajian ini membentangkan tiga teknik baharu yang mempunyai kerumitan rendah untuk mengurangkan CF dalam sistem OFDM diikuti oleh pelaksanaan perkakasan penyelakuan yang cekap daripada dua teknik ini dengan menggunakan sistem penjana FPGA Xilinx. Bahagian pertama tesis ini membentangkan teknik baharu blok pecahan antara lembarâĂŞurutan separa hantar (SBI-PTS) yang mempunyai kerumitan rendah untuk mengurangkan CF dalam sistem OFDM diikuti dengan pelaksanaan perkakasan teknik ini yang cekap dengan penyelakuan bersama menggunakan sistem penjana FPGA Xilinx.

Dalam teknik ini, pengantara lembar pecahan blok yang baharu telah dicadangkan. Ianya boleh digunakan dalam domain frekuensi sebelum jelmaan Fourier pantas songsang (IFFT) atau dalam domain masa selepas IFFT. Selain itu, skim

pengoptimuman baharu telah diperkenalkan, di mana bilangan lelaran telah dijadikan sama dengan jumlah pecahan blok sahaja yang menyebabkan pengurangan masa pemprosesan dan pengiraan yang membawa kepada pengurangan kerumitan.

Satu teknik hibrid pengurangan CF menggunakan pendaraban-penambahan yang mempunyai kerumitan rendah dan kecekapan tinggi yang baharu untuk sistem OFDM telah dibentangkan dalam bahagian ke dua tesis. Teknik ini terdiri daripada dua blok IFFT. Pertama, output kedua-dua blok IFFT adalah dibahagikan kepada empat pecahan blok, yang kemudiannya digunakan untuk menyusun semula pecahan blok dengan tambahan sifar dengan cara yang tertentu. Kemudian, satu skim pengoptimuman baharu telah diperkenalkan di mana hanya satu urutan dua fasa dan empat lelaran perlu digunakan. Analisis berangka menunjukkan bahawa teknik hibrid yang telah dicadangkan mencapai prestasi pengurangan CF yang lebih baik dengan kerumitan jauh lebih rendah serta prestasi kadar ralat bit yang lebih baik daripada teknik pengarauan (pendaraban) dan tambahan CF sedia ada. Ciri penting lain skim ini adalah ia tiada maklumat sampingan (SI) yang diperlukan untuk meningkatkan kecekapan penghantaran.

Bahagian terakhir tesis ini membentangkan satu teknik pengarauan yang mempunyai kerumitan rendah baharu untuk mengurangkan CF dalam sistem OFDM diikuti oleh pelaksanaan perkakasan penyelakuan bersama yang cekap dengan menggunakan sistem penjana FPGA Xilinx. Dalam teknik ini, output IFFT tunggal diulang sebanyak M kali dan dibahagikan kepada M pecahan blok, yang kemudiannya telah di antara lembar. Kemudian, satu skim pengoptimuman baharu telah diperkenalkan di mana hanya satu dua turutan fasa perlu digunakan. Tidak seperti C- PTS yang memerlukan blok M-IFFT dan lelaran 2^{M-1}, teknik yang dicadangkan hanya memerlukan blok IFFT tunggal dan M lelaran. Ciri ini mengurangkan masa pemprosesan dan pengiraan dengan ketara yang membawa kepada pengurangan kerumitan. Keputusan penyelakuan menunjukkan bahawa teknik baharu ini boleh mengurangkan kerumitan secara berkesan sehingga 99.95% berbanding dengan prestasi teknik PTS konvensional (C-PTS) dan menghasilkan prestasi CF yang baik.

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I certify that a Thesis Examination Committee has met on 16 March 2017 to conduct the final examination of Khalid Taher Mohammed Al-Hussaini on his thesis entitled "Design and Implementation of Low Complexity OFDM Modulator for Broadband Wireless Devices" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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6.1 Overview of the HW Co-Simulation Xilinx Implementation 152

LIST OF ABBREVIATIONS

3G	Third Generation
4G	Fourth Generation
ABC-PTS	Artificial Bee Colony
ACE	Active Constellation Extension
ACI	Adjacent Channel Interference
ADRG	Addition of Random Gaussian Signals
ADSL	Asymmetric Digital Subscriber Line
A/D	Analog to Digital Conversion
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
bps	bit per second
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
OFDM	Orthogonal Frequency Division Multiplexing
CP	Cyclic Prefix
CR	Clipping Ratio
CF	Crest Factor
D/A	Digital to Analog Conversion
DAB	Digital Audio Broadcasting
dB	decibels
dc	direct current (0 Hz)
DFT	Discrete Fourier Transform
DMT	Discrete Multi-Tone
DSI	Dummy Sequence Insertion
DSR	Dummy Subcarriers Ratio
DVB	Digital Video Broadcasting
Eb/No	Bit Energy-to-Noise Density Ratio
FDM	Frequency Division Multiplexing
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HMA	Hybrid Multiplicative-Additive CF Reduction Technique
IBO	Input Back-Off
ICI	Inter-Carrier Interference
IDRG	Insertion of Dummy Random Gaussian Subcarriers
i.i.d.	independent identically distributed
IDFT	Inverse Discrete Fourier Transform
IFFT	Inverse Fast Fourier Transform
ISI	Inter-Symbol Interference
ITU-R	International Telecommunication Union-Radio
JTAG	Joint Test Action Group
Mbps	Mega bits per second

MCM	Multi-Carrier Modulation
MDM	Multi-Dimensional Modulation
OBO	Output Back-Off
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
Parallel TS-PTS	Parallel Tabu Search
P/S	Parallel-to-Serial Conversion
PMEPR	Peak to Mean Envelope Power Ratio
PAPR	Peak to Average Power Ratio
PC-PTS	PTS-Combining PS and PE
PE-PTS	PTS-Excluding Phase rotating vectors
PRT	Peak Reduction Tones
PSD	Power Spectral Density
PS-PTS	PTS-dominant time-domain Samples selected by Pn
PSK	Phase Shift Keying
P/S	Parallel to Serial
PTS	Partial Transmit Sequences
QAM	Quadrature Amplitude Modulation
QCQP	Quadratically Constrained Quadratic Program
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RC-PTS	Reduced-Complexity-PTS
RMS	Root Mean Square
RRCF	Root Raised Cosine Filter
RS	Reed-Solomon
SBC	Sub Block Coding
SBI-PTS	Subblocks Interleaving-PTS
SC	Single Carrier
SER	Symbol Error Rate
SES	Suboptimal Exhaustive Search
SL	Soft Limiter
SLM	Selected Mapping
SLS	Successive Local Search
SNR	Signal to Noise Ratio
SoC	System on a Chip
S/P	Serial to Parallel
SSPA	Solid State Power Amplifier
SSI	Scrambling with Single IFFT CF Reduction
TI	Tone Injection
TR	Tone Reservation
VHDL	Visual Hardware Design Language
WCDMA	Wide Band Code Division Multiplexing
WLAN	Wireless Local Area Network
ZedBoard	Zynq Evaluation and Development Board

CHAPTER 1

INTRODUCTION

1.1 Background

Most of the current wireless broadband systems are based on orthogonal frequency division multiplexing (OFDM) system in order to combat intersymbol interference (ISI) caused by a fading channel (Jiang and Wu, 2008; Rahmatallah and Mohan, 2013; Han and Lee, 2005). However, OFDM is considered as one of the most significant technologies ideal for different communication and broadcasting systems (Rahmatallah and Mohan, 2013; Wang and Tellambura, 2006; Lim et al., 2009). This is because OFDM offers high spectral efficiency, robustness to frequency-selective fading, tolerant to radio channel delay spread and power efficient (Rahmatallah and Mohan, 2013; Bingham, 1990a; Koffman and Roman, 2002). Consequently, OFDM has been adopted as a standard for high data rate communications like worldwide interoperability for microwave access (WiMAX), Digital Video Broadcasting (DVB) and Long Term Evolution (LTE) (Zhang et al., 2007).

However, one major drawback of an OFDM signals is its inherent wide dynamic range between the peak and the average power called crest factor (CF) (Rahmatallah and Mohan, 2013; Chang and Gibby, 1968). This is because there are many subcarriers are in phase with each other and each of the subcarrier having different phase values. When all subcarriers are added up together, it will lead to a sudden shot up in output envelope as subcarriers attain peak value simultaneously (Weinstein and Ebert, 1971). Therefore, the contrast between the peak value and the average value in an OFDM system might be very high. The large CF causes the transmit power amplifier to enter the non-linear region, distorting the signal and resulting in a significant increase in the bit error rate (BER) at the receiver (Han and Lee, 2005; Tranter et al., 2007; Bingham, 1990b). Clearly, it is important that the CF should be reduced to ensure efficient transmissions in OFDM systems. The main criterion when designing a CF reduction scheme is to have the CF reduced to its lowest possible value and maintain its performance at the same time (Rahmatallah and Mohan, 2013).

1.2 Related Work

Aforementioned, one major drawback of an OFDM signal is its high CF. This stems essentially from the IFFT operation. In time domain, data symbols across subcarriers can be added up to produce high peaks at some instant. For example, in an OFDM system with 512 subcarriers and BPSK modulation, the PAPR at the output can be as high as 10dB. CF of 10 dB means that for transmitting an average power of 0.2W, the power amplifier should be able to handle power peaks of 2.0W which is 10 times higher. In other words, the power amplifier cannot operate efficiently and hence consumes much power for transmission (Goldsmith, 2005; Tarokh and Jafarkhani, 2000a).

Numerous CF reduction techniques have been proposed to reduce the CF (Lim et al., 2009). These techniques can be classified into signal scrambling (multiplicative) techniques such as selective mapping (SLM) (Bauml et al., 1996) and partial transmit sequence (PTS) (Muller and Huber, 1997) and additive techniques such as tone reservation (TR) (Tellado, 2000), tone injection (TI) (Tellado and CiofïňĄ, 1998), peak cancellation (Ochiai and Imai, 2000), and clipping and filtering (O'Neill and Lopes, 1995).

PTS technique is the most attractive technique in multiplicative techniques because it is a distortion-less technique and offers good CF reduction performance (Rahmatallah and Mohan, 2013; Lim et al., 2009; Muller and Huber, 1997). In the PTS technique based on the phase optimization approach, the given phases are manipulated to reduce the peak of the OFDM signals to an acceptable level. Therefore, PTS is a distortion-less technique for CF reduction (Koffman and Roman, 2002; Muller and Huber, 1997). The main problems in the PTS (multiplicative) technique is that the complexity and it requires sending of side information to the receiver (Lim et al., 2009; Muller and Huber, 1997; Schwartz, 2005).

TR and TI are an efficient additive technique to reduce CF in multicarrier systems (Rahmatallah and Mohan, 2013; Han and Lee, 2005; Lim et al., 2009). TR technique is based on adding data block dependent signals to the original multicarrier signals to reduce their peaks (Rahmatallah and Mohan, 2013; Tellado, 2000; Tellado and CiofïňĄ, 1998). The added signals are computed at the transmitter and stripped off at the receiver. The added signals are dummy signals holding no information (Lim et al., 2009; Tellado, 2000). Therefore, the TR technique is also known as the dummy sequence insertion technique. The main problems in the TR and TI (additive) technique are that the computational complexity and TI needs side information required by the receiver (Rahmatallah and Mohan, 2013; Lim et al., 2009).

The computational complexity is not only troublesome for software simulation, but also hardware implementation on field programmable gate array (FPGA) (Lim et al., 2009).

1.3 Problem Statement and Objectives

OFDM is considered to be one of the important multicarrier standards in wireless communication systems. However, high CF is the major problem of OFDM, which impacts on the power efficiency and BER performance hence increases the complexity of OFDM implementation, which results in costly hardware and complex systems. Therefore to reduce the complexity of the hardware design, it has become necessary to offer an efficient and low complexity CF reduction technique (Rahmatallah and Mohan, 2013; Lim et al., 2009).

Several techniques have been proposed over the past few decades to mitigate this problem, but all of them incur various costs in the form of transmission efficiency, average transmission power, and computational complexity (Rahmatallah and Mohan, 2013; Jiang and Wu, 2008; Lim et al., 2009). In general, the most popular CF reduction techniques are the multiplicative (scrambling) CF reduction techniques (especially PTS) and additive CF technique (especially TR) both can lessen CF significantly without distorting the output. However, multiplicative and additive CF techniques are computationally more complex than others, thus limiting its implementation in OFDM having large. However, in order to demonstrate how it would perform in a realistic system, a prototype has to be built (Rahmatallah and Mohan, 2013; Lim et al., 2009; Wu and Zou, 1995).

In this thesis, the problem of high CF and its effects on the power efficiency and BER performance of the OFDM systems is analyzed. The main objective of this thesis is to design new efficient and low complexity multiplicative and additive techniques for reducing CF in OFDM systems followed by an efficient hardware co-simulation implementation by using a Xilinx system generator on an FPGA.

In particular, the following three main significant objectives have been achieved through this thesis:

- To design and implement a new low complexity high-efficiency CF scheme based on the multiplicative (scrambling) PTS scheme on FPGA.

- To design a new low complexity high-efficiency CF scheme based on the multiplicative (scrambling) and additive CF schemes.

- To design and implement a new low complexity high-efficiency CF scheme with single IFFT modulator based on the multiplicative (scrambling) scheme on FPGA.

1.4 Research Methodology

In this thesis, the CF reduction schemes are all designed, performed, and implemented at the physical layer of the OFDM systems. The most important physical

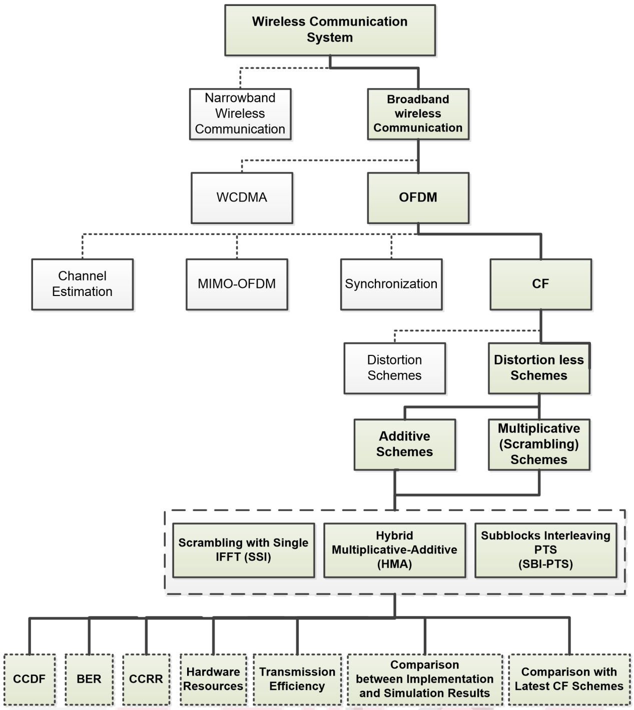

Figure 1.1: Study Module

metrics of the system namely, CCDF, BER, CCRR, and hardware resources have been used to evaluate the proposed schemes as shown in Figure 1.1 .

The first proposed CF reduction scheme is based on PTS scheme. In this scheme, a new PTS technique has been designed and followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on an FPGA. It uses a new subblocks interleaving (SBI) and optimization scheme in which only a single two-phase sequence and M iterations are required. Both SBI and optimization schemes are applied to reduce the computational complexity associated with weighting factors and also to reduce the CF and BER. In this manner, a minimal CF can be obtained with the need for M iterations, which conserves processing time and demands fewer computational resources, thus leading to lower complexity. Above all, this scheme does not require side information and therefore offers increased transmission efficiency. Hence, compared with other PTS techniques, SBI-PTS has been shown to be less complex and less resource consuming, while offering superior CF reduction performance. The FPGA implementation of this method has been discussed and it has been shown that its CF performance is comparable with the simulation results. The details of this stage are analyzed and explained in Chapter 3.

The second proposed CF reduction scheme is based on hybrid multiplicative and additive (HMA) CF schemes. It consists of two IFFT modulators. In this scheme, a new partitioning and optimization schemes are established. In partitioning scheme, the output of the two IFFT modulators is partitioned into four subblocks, which are subsequently used to rearrange the subblocks with padding zeros in a specific manner. In optimization scheme, only a two-phase sequence is required with only four iterations. Numerical analysis shows that the proposed hybrid technique achieves better CF reduction performance with significantly lower complexity and better bit error rate performance than the existing multiplicative and additive CF techniques. The details of this stage are analyzed and explained in Chapter 4.

The last proposed CF reduction scheme is based on multiplicative (scrambling) CF schemes. It has been designed and followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on an FPGA. It is using a single scrambling IFFT (SSI) modulator and new optimization scheme in which only a two-phase sequence is required. Two reordering methods and optimization schemes are applied to reduce the computational complexity of the weighting factors and decrease CF. By this means, a low CF can be achieved needing only M iterations, which consumes lower computational resources, thus leading to lower complexity. Compared against other latest multiplicative schemes, this scheme shows especially low complexity and resource consumption while offering a superior CF reduction performance. The main features of the proposed technique are that it only needs one IFFT and M iterations; complexity is thus significantly reduced. Compared with other CF reduction schemes, the proposed scheme is the most unique and exhibits the best performance. Through the comparison of performance between simulation and hardware, it is distinctly illustrated that the designed hardware block diagram is as workable as the simulation and the difference of the result is only 0.1 dB. The details of this stage are analyzed and explained in Chapter 5.

1.5 Thesis Contribution

Based on the objectives stated above, this thesis introduces new contributions in the area of the broadband wireless communication system and FPGA implementation over OFDM systems. The main aim is to design and implement high-efficiency low-complexity CF reduction techniques of the OFDM systems through the following contributions:

- *A New PTS Technique with High Efficiency and Low Complexity.*

  The new high efficiency and low complexity SBI-PTS technique, which is designed and followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on FPGA in Chapter 3. It is different from the conventional PTS (C-PTS). Compared with other PTS techniques, SBI-PTS has been shown to be less complex and less resource consuming respectively while offering superior CF reduction performance. Above all, this technique does not require side information and therefore offers increased transmission efficiency.

- *A New Hybrid Technique Based on Multiplicative-Additive Scheme.*

  According to the HMA algorithm developed in Chapter 4, this technique consists of two IFFT blocks. The input symbols of the first IFFT are the mapped symbols, whereas the input symbols of the second IFFT are the summations of the absolute value of the real part of the outer signal constellation points and zeros symbols. The HMA technique achieves better CF reduction performance with significantly lower complexity and better BER performance than the existing scrambling (multiplicative) and additive CF techniques.

- *A New Single IFF Technique Based on Multiplicative (Scrambling) Scheme.*

  According to the SSI algorithm developed in Chapter 5, this technique consists of a single IFFT block. In this technique, two re-ordering methods are proposed. In the first one, the output of a single IFFT modulator is divided into Q subblocks, which are subsequently duplicated and re-ordered in a specific manner. In the second one, the output of a single IFFT modulator is partitioned into Q subblocks, which are subsequently duplicated and interleaved into M subblocks. Unlike the C-PTS which needs M-IFFT blocks and W^{M-1} iterations, the proposed technique requires only a single IFFT block and M iterations. The results demonstrate that the new technique can effectively reduce the complexity up to 99.95% compared with the C-PTS technique and yields good CF performance.

- *Reducing the Processing Time and Less Computation by Using the New Optimization Method.*

  A new low complexity optimization method has been applied for all proposed techniques at the transmitter side. The method is called truth table candidates cancellation (TTCC), that obviates multiplicative operations is applied. Only a two-phase sequences, where the possible phases are $\{0; 1\}$ are required and in which the number of iterations is made to be equal to the number of subblocks only which results in reduced processing time and less computation that leads to reduced complexity. It can be applied in all Multiplicative-additive CF schemes.

- *Transmission Efficiency Increase by Using a New Side Information Detection Method.*

  A new low complexity optimization method has been applied for all proposed techniques at the receiver side. It can be applied in all multiplicative-additive CF schemes. In this method, the first samples of the OFDM symbol are tested to determine the minimum sample power among them, identify its index, and insert this index into the encoder that is similar to that at the transmitter to generate the phase sequence. Thus, the proposed techniques do not require the sending of side information and therefore offers increased transmission efficiency.

- *Better CF and BER performances by Using a New IQ Parallel Interleaver.*

  The subblocks interleaving is used a new IQ parallel interleaving scheme which is developed in Chapter 3. It can be applied in all Multiplicative-additive CF schemes. The new subblocks interleaving is adopted mainly to reduce CF by limiting the probability that two peaks are combined which would increase the output envelope abruptly. The data interleaving process combines some high peaks with low peaks which will neutralize each other and hence reducing the probability occurrence of high CF redution and at the same time decrease BER.

- *A Simple Subblock Rearrangement Approach.*

  A new simple rearrangement approach is introduced in Chapter 4 and 5, in which, the outputs of multiple/single N-point IFFT are partitioned/divided into subblocks. Then, the subblocks are re-ordered with padding zeros. By using this combination, this signal can be reconstructed easily at the receiver, the long correlation patterns would be broken down; as a result, the CF will be reduced.

- *Achieving the Best CF, CCRR, and BER Compared to Latest Works*

  All proposed schemes developed in Chapter 3, 4 and 5 have achieved good CF redction, CCRR, and BER compared with the conventional and latest multiplicative-additive schemes. In these schemes, the low complexity optimization, IO parallel interleaving, and rearrangement schemes are applied to reduce the computational complexity associated with weighting factors and also to reduce the CF and BER. In this manner, a minimal CF can be obtained with the need for M iterations, which conserves processing time and demands fewer computational resources, thus leading to lower complexity.

- *Significant Reduction in the Hardware Complexity by Wisely Utilize Hardware Resources in FPGA.*

  The Performance of FPGA implementation can be evaluated through hardware resource being used to carry out the respective approach. In this case, the less amount of hardware resource being used indicated higher performance for the respective .approach. All implementation is performed online, including the phase sequence optimization and CF calculations for all candidate phase sequence. Compared with the available implemented CF techniques, the hardware resources of the proposed schemes have the best reduction.

1.6 Research Scope

As illustrated in Figure 1.2, the research scope is divided into two main parts namely, design and hardware implementation. The design part includes the complexity analysis and simulation modeling.

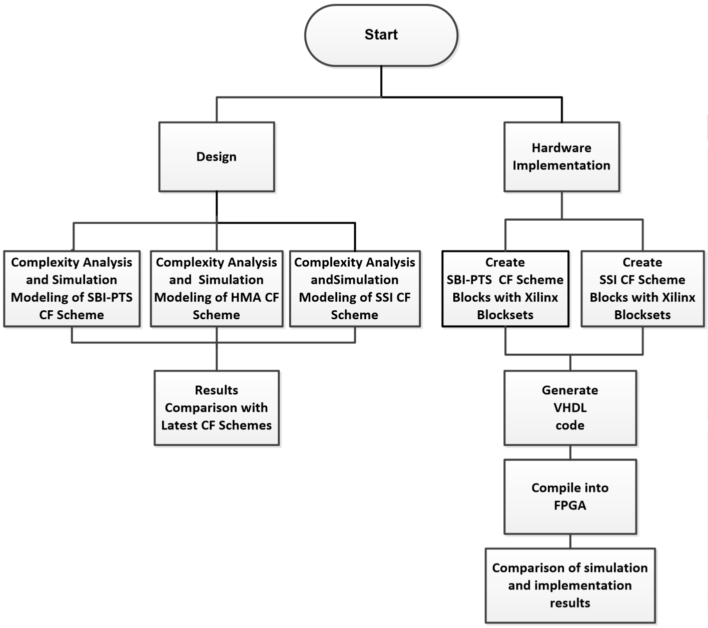

Figure 1.2: Flow Chart of the Research Scope

In Complexity analysis and design, the three novel CF reduction (SBI-PTS, HMA, SSI) techniques, which are based on multiplicative-additive CF reduction concepts are analyzed and the results are compared with the conventional and latest CF reduction techniques. These new techniques are simulated by using Matlab simulation. After successfully simulate the new CF techniques, the most significant metrics are used for comparison with the conventional and latest CF reduction techniques.

In the hardware implementation, the SBI-PTS and SSI CF techniques are implemented in FPGA using MathWorks/Simulink DSP tools with Xilinx blocks which are called hardware co-simulation. First, the simulation is transferred into Xilinx blocks and then by using Xilinx system generator, the simulation is translated to VHDL codes. The CF techniques implementation includes all the blocks of the proposed techniques. After the CF technique blocks are created, it can be compiled into FPGA. Also, the joint test action group (JTAG) block is created to test the CF in real time.

1.7 Significance of the Study

The power amplifier (PA) is one of the most costly parts of the communication systems; hence the optimum usage of its gain is needed. It is well known that PA has nonlinear characteristics and a limited linear region so, if the PA works in the nonlinear region, it causes out-of-band as well as in-band distortion, which wastes a lot of energy and as a result reduces battery life (Rahmatallah and Mohan, 2013; Lim et al., 2009; Koffman and Roman, 2002). This also causes unnecessary emission which also harms the environment. Also, it causes interference with adjacent channels (hence the other users). When the introduced signal has high CF, back-off in the PA becomes necessary (Sharif and Khalaj, 2001; Ermolova, 2001). In this case, transmitted signal never drive the PA into the nonlinear region or PA has to have a large dynamic range in order to prevent any signal distortion.

In many low-cost mobile device applications, the drawback of high CF may outweigh all the potential benefits of broadband communication systems. High CF may have a deleterious effect on battery lifetime on mobile devices. So applying low complexity high-efficiency technique in recent communications standard such as WiMAX, LTE, and 4G/5G will significantly reduce the complexity of those systems and bring down the cost of the system. The CF reduction technique maximizes power efficiency which results in prolonged battery life (Rahmatallah and Mohan, 2013; Lim et al., 2009; Weinstein and Ebert, 1971).

1.8 Thesis Organization

This thesis covers the principles of OFDM concentrating on the CF problem in OFDM systems and contains six chapters. The thesis is organized as follows:

In **Chapter 1** provides an introduction to the CF problem in OFDM systems, statement of the problem and the objectives, the research methodologies of the proposed techniques, and the significant of the study, scope, and thesis contributions.

Chapter 2 gives a review of OFDM systems and CF problem as it is the main research issue in this work. The chapter starts with the background of the OFDM systems, advantages, and disadvantages of OFDM, mathematical models of OFDM systems, and analysis of OFDM signals. PA and sensitivity of OFDM to non-linear characteristics of PA, CF problem in OFDM systems, statistical properties of CF in OFDM systems, design specifications for CF reduction technique and the use of interleaving and permutation to improve CF. In addition, the parameters affecting CF, the essential features in CF reduction technique, classification of existing CF reduction technique and the FPGA implementation of CF reduction techniques are described and their performances are discussed.

Chapters 3, 4, and 5 introduce the proposed techniques of this research work. Multiplicative (scrambling) and additive CF reduction techniques, and their FPGA implantations are all described in these chapters.

In **Chapter 3** presents the proposed subblocks interleaving PTS (SBI-PTS) CF reduction technique. The mathematical model and simulations outputs analysis are given for SBI-PTS technique and is followed by the description of the hardware co-simulation implementation of this technique that is done by using a Xilinx system generator on FPGA. The pivotal metrics such as CCDF, BER, CCRR and the hardware resources being used and the comparison with latest existing CF reduction technique are also given in this chapter.

Chapter 4 introduces new low complexity high-efficiency hybrid multiplicative-additive (HMA) CF reduction technique starting with the analysis of a mathematical model for attractive multiplicative and additive CF reduction technique. Then, the simulations outputs analysis are presented and discussed. The significant metrics such as CCDF, BER, CCRR and the comparison with latest existing CF reduction technique are also introduced in this chapter.

In Chapter 5 presents new single IFFT scrambling (SSI) CF reduction technique. The mathematical model and simulations outputs analysis are given for SSI technique and is followed by the description of the hardware co-simulation implementation of this technique that is done by using a Xilinx system generator on FPGA. The pivotal metrics such as CCDF, BER, CCRR and the hardware resources being used and the comparison with latest existing CF reduction technique are also given in this chapter.

In Chapter 6 the thesis is summarized, followed by the discussion of the research applicability and limitations. Then, several research issues and directions are suggested for further investigation.

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