



UNIVERSITI PUTRA MALAYSIA

***LOW POWER TEXT COMPRESSION USING HUFFMAN CODING WITH
POWER MANAGEMENT CONTROLLER***

MAAN HAMEED MOHAMMED

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**LOW POWER TEXT COMPRESSION USING HUFFMAN CODING WITH
POWER MANAGEMENT CONTROLLER**

By

MAAN HAMEED MOHAMMED

**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia
in Fulfillment of the Requirements for the Degree of Master of Science**

April 2016

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DEDICATION

This thesis dedicated to

All I love

Specially

My dearest parents

My beloved wife

For their endless encouragement, patience, and support and for being a great source of motivation and inspiration

All my friends

And to my homeland, Ira



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UPM

Abstract of thesis presented to the senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

**LOW POWER TEXT COMPRESSION USING HUFFMAN CODING WITH
POWER MANAGEMENT CONTROLLER**

By

MAAN HAMEED

April 2016

Chairman : Assoc. Prof. Abd. Rahman Ramli., PhD
Faculty : Engineering

Data compression with low power dissipation is a useful technique in digital systems because it reduces data size with the smallest power consumed to overcome the design limitations. Huffman lossless compression is an important technique in information theory as well as in today's IT field. Reducing data size is the most important goal for Application-Specific Integrated Circuit (ASIC) design and power consumption is one of important issues which restrict the design performance. Therefore, reducing data size and embedding a Power Management Controller (PMC) in a synchronous system is a suitable technique for this problem. Using PMC to control the system to operate in fast and slow modes leads to low power dissipation. This work focused on the design of high performance Huffman compression with low power technique for all English text. Huffman tree is generated by sorting data according to their frequencies and traversing the tree to extract codeword bits for each character. Verilog HDL language used for writing Huffman codes and ModelSim tool was used for simulating the functionality of Huffman. In addition, Field-Programmable Gate Array (FPGA) was used to verify the functionality of Huffman. 8 green LEDs on the FPGA board were used as ASCII input for Huffman encoder, while the first 9 red LEDs on the board were utilized as output of the encoder. The process is reversed in the decoder implementation. A new sub module named PMC was created using clock gating and frequency scaling to improve power consumption in flexible design. Furthermore, Synopsys power compiler with 130nm technology library was used for power analysis. In this study, data size was reduced to 47.95% after compression process when compared with original data size. Moreover, with using PMC, power consumption was reduced up to 52.52% when compared with Huffman without using PMC.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

**PEMAMPATAN TEKS BERKUASA RENDAH MENGGUNAKAN TEKNIK
PENGEKODAN HUFFMAN BESERTA PENGURUSAN KAWALAN KUASA**

Oleh

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Pemampatan data dengan pengurangan kuasa rendah adalah satu teknik yang berguna dalam sistem digital kerana ia mengurangkan saiz data dengan kuasa yang paling kecil yang digunakan untuk mengatasi had reka bentuk. Teknik mampatan tanpa hilang Huffman adalah satu teknik penting dalam teori maklumat dan juga dalam bidang IT hari ini. Pengurangan saiz data adalah perkara paling penting dalam reka bentuk ASIC (Spesifik Aplikasi Litar Bersepadu) dan juga pengurangan kuasa merupakan faktor utama yang menyekat prestasi reka bentuk. Oleh itu, dengan pengurangan saiz data dan penggunaan Pengurusan Kawalan Kuasa (PMC) dalam sistem segerak adalah teknik yang sesuai bagi menyelesaikan masalah ini. Dengan menggunakan teknik PMC ini untuk, sistem mengawal dalam mode pantas dan juga lambat dapat mengurangkan kuasa pelepasan beroperasi. Kerja ini memfokuskan kepada pembangunan prestasi teknik pemampatan teknik Huffman dengan penggunaan kuasa rendah pada kesemua teks Inggeris. Pohon Huffman dijanakan dengan teknik isihan data mengikut frekuensi mereka dan menyusuri pepohon tersebut untuk mengekstrak bit-bit per kata kod bagi setiap aksara. Bahasa HDL Verilog telah digunakan untuk menulis modul-modul kod Huffman, and alat Model Sim telah digunakan untuk simulasi bagi mencapai kefungsi rekabentuk Huffman. Kemudian, pelaksanaan Tatasusunan Get Aturcara Medan (FPGA) telah digunakan bagi mengesahkan fungsi Huffman. Proses tersebut telah menggunakan 8 LED hijau dalam papan FPGA sebagai input ASCII untuk pengekod Huffman. 8 LED hijau di papan FPGA digunakan sebagai input ASCII untuk Huffman pengekod, manakala 9 LED merah yang pertama di atas papan telah digunakan sebagai output pengekod. Proses ini bertukar arah pada pelaksanaan penyahkod. Satu modul sub baru yang dinamakan PMC telah dicipta menggunakan penggetan jam dan skala kekerapan untuk meningkatkan penggunaan kuasa dalam reka bentuk yang fleksibel. Tambahan pula, pengkompil kuasa Synopsys dengan perpustakaan teknologi 130nm telah digunakan untuk analisis kuasa. Dalam kajian ini, saiz data telah dikurangkan kepada 47.95% selepas proses mampatan berbanding saiz asal. Malahan, dengan menggunakan PMC, penggunaan kuasa telah dikurangkan sehingga 52,52% berbanding Huffman tanpa menggunakan PMC.

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Most importantly, I want to say thanks to my dearest parents, my beloved wife, and my family. Who helped me out of many difficulties in life and provided me with warm encouragement.

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LIST OF ABBREVIATIONS

ASIC	Application-Specific Integrated Circuit
AVS	Adaptive Voltage Scaling
ATE	Automatic Test Equipment
ALU	Arithmetic Logical Unit
ADL	Architecture Description Languages
AAT	Actual Arrival Times
CR	Compression Rate
CODEC	Coding and Decoding
CAFD	Cycle-Accurate Functional Description
CW	Code Words
CMOS	Complementary Metal Oxide Semiconductor
CG	Clock Gating
CAFD	Cycle-Accurate Functional Description
CAD	Computer-Aided Design
DVS	Dynamic Voltage Scaling
DVFS	Dynamic Voltage and Frequency Scaling
DE	Development and Education
DSP	Digital Signal Processing
DC	Design Compiler
EDA	Electronic Design Automation
E_D	Encoder-Decoder
FPGA	Field-Programmable Gate Array
FIFO	First In First Out
GC_enc	Encoder Clock Gating
GC_dec	Decoder Clock Gating
HDL	Hardware Description Language
HLS	High Level Synthesis
H_S	HIGH – Slow
IP	Intellectual Property
IT	Information Technology
IC	Integrated Circuit
ITRS	International Technology Road map for Semiconductors
ICG	Integrated Clock Gating
LZW	Lempel Zev Welch Algorithm
LFSR	Linear Feedback Shift Register
LUT	Look Up Table

LSB	Least Significant Bit
LIFO	Last-In, First-Out
MVS	Multi-Level Voltage Scaling
MSV	Multiple Supply Voltages
MCD	Master Clock Divider
POFSCG	Power Optimization Frequency Scaling Clock Gating
PC	Personal Computer
PSO	Power Gating or Power Shut-Off
PLL	Phase Locked Loop
PLI	Programming Language Interface
PRBS	Pseudo Random Binary Sequence
PMC	Power Management Control
POFSCG_enc	Power Optimization Frequency Scaling Clock Gating Encoder
POFSCG_dec	Power Optimization Frequency Scaling Clock Gating Decoder
RISC	Reduced Instruction Set Computing
RTL	Register Transfer Level
RLE	Run Length Encoding
RATs	Required Arrival Times
SoC	System on Chip
SVS	Static Voltage Scaling
SRPG	State Retention Power Gating
S&RPG	Save and Restore Power Gating
STA	Static Timing Analysis
TSPC	True Single Phase Clock
THP	Total Huffman Power
TPE	Total Power Encoder
TPD	Total Power Decoder
TP_PMC	Total Power PMC
TPE_SM	Total Power Encoder Slow Mode (top-level)
TLPD_off	Total Leakage Power Decoder (off)
TPE_HP	Total Power Encoder High Performance (top-level)
TPD_SM	Total Power Decoder Slow Mode (top-level)
TLPE_off	Total Leakage Power Encoder (off)
TPD_HP	Total Power Decoder High Performance (top-level)
VLSI	Very Large Scale Integration
VLC	Variable Length Codes
WSA	Wide Spread Adapting

CHAPTER 1

INTRODUCTION

The demand for data compression and low power consumption are motivated by several factors such as the evolution of portable design, reliability effects, and flexibility. The evolution of portable tools such as smartphones and laptops are the necessary portion driving the demand for combining these two goals data compression and low power consumption in the design. The need for the portable device is growing each year and is forecasted to grow more in the future. Right from beginning, human beings have always in the need of communication means. Moreover, technology has led to evolution of the best systems that have made life generally easier. In recent decades, there has been explosion of evolution of devices and services which has led to faster and more reliable growth and development of digital designs. These are possible because portable electronic devices have become more robust with increase in computing capability and improvements in communication speed and reliability. However, all the increases in speed and reliability have challenges. Two of the most important challenges are data compression and power consumption. Reduced data size leads to decreases in the amount of area needed for data storage. The reduction is achieved by removing redundant data. The purpose of data compression is to present original data source in digital structure including fewer bits as possible while meeting the smallest necessity of reproducing original data. Processing small data size definitely consumes less power than large size because the power needed for transmitting and storing the new size is less than the original file size.

Furthermore, recently larger and more efficient batteries are being used to solve excessive power consumption problem. Therefore, in the modern days economic and environmental issues have forced the researchers to think on improvement and discovering solutions for reducing power consumption and increasing reliability in digital designs. This task was improved in relation with the library of Synopsys power compiler and it goals to studying the practicing and evaluating digital design techniques for data compression and reducing power consumption. The design flow constructed with Synopsys EDA (electronic design automation) tools and 130 nm technology libraries which are currently used for mature products to implement all software and hardware in Huffman design for data compression. Huffman design based on binary tree used for downsizing data is a useful compression technique for reference symbols that are not uniformly probable. It produces the lowest probable quantity of code symbols per source symbol. The lossless manner of compression and decompression process utilize a simple coding called Huffman coding is adopt in text data involves all characters of English language.

Clock gating as the name proposed, is employed to inactive clock signal that supports sequential blocks in digital design during theirs registers are not being used. This method enables reduction of switching activity answerable for the major a portion of the general power dissipation which is due to the charge/discharge of the

load capacitance named dynamic power. Moreover, clock gating is one of the most important methods used for decreasing power dissipation in digital circuits. The prime idea is to stop clock in the parts of the design that are idle at a given period to decrease switching activity in the registers and transfer the data from those registers for considerable power saving. Frequency scaling is used to divide the master clock into sub-modules in the design and make each of them work on fast and slow mode. The implementation of frequency scaling involves start of added logic unit to gate the clock and this style is utilized to reduce switching activity.

Furthermore, there will be creation of good chance to meet and deal with business environments, advanced technologies and state of the art EDA tools with integration of a system team from one of the world's brains in EDA tools. Unnecessary power consumption in IC complicates their use in portable systems. This also causes high temperatures which lowers the quality of device and decrease chip lifetime (Uppalapati, 2004). The demands of consumers for more functionality with high performance lead to generation of high temperatures, because high performance need to high frequency, while not all the data need the same frequency for execution, part of data need low frequency implementation. Therefore, putting the design to working in one frequency leads to high temperature and decrease a chip lifetime. Therefore, power consumption of digital system has become more important that the designers spend significant amount of their time optimizing their designs for minimal power consumption (Shinde & Salankar, 2011). Sequential design consumes large amount of power because the clock signal switches at all times. Additionally, clock signal tends to be over loaded (Dev, et al., 2013).

Moreover, reduction of power consumption does not only lengthen the battery life time in portable device, smart phones or the entire modern devices but it also increase the reliability by decreasing the overhead which is very important in keeping the design stable without overheating (Nejat, et al., 2013). The target is to keep the temperature low to avoid design restrictions. The methodology of achieving this aim is to have the performance when it is required only. The researchers are looking for the best technologies to reduce power without degrading to the performance (Sahni, et al., 2014).

Huffman coding with low power design are keys for data compression and power reduction techniques used by many designers. Moreover, it is one of the multiple well-known low-power systems which are very efficient in decrease power dissipation in digital design. The purpose of clock gating is inactive or suppresses change to parts of the clock path like flip-flop, clock network and logic under a certain condition computed by clock gating circuits (Shinde & Salankar, 2011). In other word, the clock is disabled when it is not necessary in clock gating to reduce power consumption. Clock gating simply switches off the clock where it unnecessarily consumes power. By following the stated procedure, the power consumption becomes less up to half without affecting the performance of the design (Sahni, et al., 2014). To control temperature levels, the chip needs specialized and costly packing and cooling arrangements which would result in the future escalation of the system cost. The growing need for portable communication device and

computing system has increased the need for optimization of power consumption in the chip. Overall low-power design is a critical technology needed in semiconductor industry today.

1.1. Problem Statement

Data compression with low power consumption is a useful technique in a digital system. Reducing data size is the most important goal for ASIC design, and power consumption is one of the common popular issues which restrict the design performance. Power dissipation can be reduced by keeping memory resources in a small size. One way to achieve this goal without affecting the performance is to employ data compression. Hence, data compression with low power dissipation is the suitable way to overcome these problems. Therefore, this work aims to design Huffman compression for all English alphabets based on binary tree. Furthermore, proposing a novel method for low power techniques to decrease power consumption in the design, targeting to overcome the main drawback of Huffman design that the overhead generated from coding and decoding process (JensMabberg, 2015). Therefore, reducing the power dissipation is one of the most important goals of digital system. The goal of using clock gating and frequency scaling for low power design is to propose a novel method for achieving the flexibility of design by allowing each module work in fast and slow modes (Kulkarn., R, and Kulkarni., S.Y, 2014). This method takes into account the characteristics of system requirements. Finally, this research aims to design Huffman coding for compression decompression process with proposing a Power Optimization Frequency Scaling and Clock Gating (POFSCG). In this work, clock signal was generated by combining two knobs of power optimization to reduce power consumption and realize flexibility of design.

1.2. Research Aim and Objectives

This thesis aims to develop an improved data compression with low power consumption and flexibility of digital design. The objectives of this research are to:

- 1- Design and implement Huffman coding for English text compression.
- 2- Design and implement a low power management sub module for clock gating and frequency scaling in standard Huffman design.
- 3- Evaluate the performance of Huffman design to achieve the smallest size of data compression with reduced power consumption to get the best results in data compression and power consumption.

1.3. Scope of the Study

In this work, the proposed Huffman for data compression and low power consumption was introduced. The main parameter used to achieve data compression was the frequency of the data used, while the main parameter in low power techniques was the frequency for the clock signal (Jacobson, et al., 2005). Therefore, frequency constituted the main constraint to the design. Type of data used in compression and decompression processes was text data. Evaluation of performance

was achieved by compressing the data using Huffman coding based on binary tree and dynamic power using low power techniques. In this case, there was decrease in clock frequency in sub-system design level to allow each module work on its own frequency. Different levels of frequency for clock signal were tested and the results were combined to get the final performance of the design. From the evaluation results, it was clear that low power design based on clock gating and frequency scaling was the best combination to achieve reliability and low power consumption.

The proposed design was achieved by using ASIC and FPGA design methodologies. In order to implement encoder and decoder architectures, 130 nm Silterra libraries with Synopsys power compiler provided by the Universiti Putra Malaysia was used to evaluate the performance of the design. The architectures of compression and decompression algorithm design were created using Verilog HDL language (Quartus II 11.1 Web Edition (32-Bit)). In addition to that, simulation was achieved by using ModelSim-Altera 10.0c (Quartus II 11.1) Starter Edition.

1.4. Contribution of This Research

The framework proposed can handle large amount of data size and minimize power consumption for development system. The suggested techniques designed to improve data size and power dissipation. Compression process to deals with large data size, and proposed a new sub-module was a combination of two techniques of low power design. Clock gating and frequency scaling were used to achieve low power consumption of Huffman design to enable each module have fast and slow modes. A convenient way to do that is to adjust the frequency using a divider version of the master clock. The reason for that was that the system could achieve low power consumption by allowing each sub-system to operate on its own frequency to avoid high frequency just when the system was required.

1.5. Outline of Thesis

The organization of the remaining chapters of thesis is as follows:

Chapter Two introduces readers with various ideas in data compression and low power design and introduces different approaches in building Huffman with low power design. In the other part of this chapter, various virtualization techniques were presented and explained.

Chapter Three dealt with the methodology of research and discussed the prim idea with method related to the application of various strategies to implicit data compression with low power dissipation. Steps involved in the design for low power consumption and high performance were discussed and the readers were introduced to the methods used.

Chapter Four (results and discussion) presented the results of simulation study. This chapter dealt with evaluation of the compressed data size and power consumption with highlighted the performance figures of different developed methods. In this chapter, the developed design was compared with other methods in the literature to show its betterment and weaknesses.

Chapter Five (conclusion of the dissertation) summarized the results and proposed further research for future developments. The Appendix was for additional materials, Verilog HDL function and script files written in the course of the research.



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