UNIVERSITI PUTRA MALAYSIA

A COMPLEXITY-REDUCED DIGITAL PREDISTORTION FOR RADIO FREQUENCY POWER AMPLIFIER

SIBA MONTHER YOUSIF

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By

SIBA MONTHER YOUSIF

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

June 2016

DEDICATION

This work is dedicated to:

The memory of my precious Father

My darling Mother

My dear Husband and Brother

&

My beloved Daughters, Dalia and Meena

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the Degree of Doctor of Philosophy

A COMPLEXITY-REDUCED DIGITAL PREDISTORTION FOR RADIO FREQUENCY POWER AMPLIFIER

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June 2016

Chairman : Assoc. Prof. Roslina Mohd. Sidek, PhD
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Power amplifier (PA) is a major source of nonlinearity in a communication system since it often has to operate close to the saturation region to achieve high power efficiency. The nonlinearity includes out-of-band emission which causes adjacent channel interference and in-band distortion that degrades the bit error rate performance. In modern high speed communications, transmission schemes with high spectral efficiency such as Code Division Multiple Access (CDMA) and Orthogonal Frequency Division Multiplexing (OFDM) are more sensitive to PA nonlinearity and memory effects. In order to overcome the conflict between the linearity and the power efficiency of the PA, a linearization technique is required. One of the most cost-effective linearization techniques is Digital Pre-Distortion (DPD). The main justification for a DPD is to improve PA efficiency since PA is the most power consuming device in a transmitter. However, high complexity DPD leads to high power consumption due to intensive processing. Therefore, it is essential that the power saved by using DPD is not spent on a high complexity DPD algorithm.

In this thesis, a low-complexity DPD model is proposed, verified, and experimentally evaluated for linearizing power amplifiers with memory effects. The proposed model derived from Volterra-series includes three parallel dynamic branches. This proposed model is constructed by treating the linear and nonlinear memory effects separately, which will provide an effective way to present efficient distortion compensation with low-complexity for PA linearization. The performance of the proposed model is assessed using a commercial class-AB power amplifier driven by a 2-carrier Wideband CDMA (WCDMA) signal of 15 MHz bandwidth and Long-Term Evolution (LTE) signals of 15 MHz and 20 MHz bandwidth. The simulation and experimental results show that the proposed model outperforms the MP model in terms of Adjacent Channel Leakage power Ratio (ACLR) performance by 7 dB and 6 dB, respectively for the 15 MHz bandwidth and by 6.8 dB and 6.5 dB, respectively for the 20 MHz bandwidth. These results were achieved with a reduction in the complexity by 16% in terms of number of floating point operations (FLOPs) as compared to the MP's model complexity. This work demonstrates that a high linearity performance was achieved while the computational complexity of the proposed DPD model was minimized. These improvements will lead to reduction in transmitter power consumption and also reduction in hardware resources required for on-chip DPD implementation.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk Ijazah Doktor Falsafah

PRAHEROTAN DIGIT KURANG KEKOMPLEKSAN UNTUK PENGUAT KUASA FREKUENSI RADIO

Oleh

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Pengerusi : Prof. Madya Roslina Mohd. Sidek, PhD
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Penguat kuasa (PA) adalah sumber utama ketaklelurusan dalam sistem komunikasi kerana sering beroperasi berhampiran dengan kawasan tepu untuk mencapai kecekapan kuasa yang tinggi. Ketaklelurusan tersebut merangkumi pancaran luar jalur yang menyebabkan gangguan saluran bersebelahan dan herotan dalam jalur yang menurunkan prestasi kadar ralat bit. Dalam komunikasi moden berkelajuan tinggi, skim penghantaran dengan kecekapan spektrum tinggi seperti Code Division Multiple Access (CDMA) dan Orthogonal Frequency Division Multiplexing (OFDM) adalah lebih sensitif kepada ketaklelurusan dan kesan memori PA. Dalam usaha untuk mengatasi konflik di antara kelelurusan dan kecekapan kuasa PA, teknik pelelurusan diperlukan. Salah satu teknik pelelurusan yang efektif dari segi kos adalah praherotan digit (DPD). Justifikasi utama bagi teknik DPD adalah untuk memperbaiki kecekapan PA kerana PA merupakan peranti yang menggunakan kuasa yang paling tinggi dalam penghantar. Walaubagaimanapun, DPD yang kompleks boleh meningkatkan penggunaan kuasa disebabkan pemprosesan yang intensif. Oleh itu, adalah penting bahawa penjimatan kuasa oleh DPD tidak disia-siakan pada algoritma DPD yang kompleks.

Dalam tesis ini, satu model DPD dengan kekompleksan yang rendah dicadangkan, disahkan, dan dinilai secara eksperimen untuk meleluruskan penguat kuasa dengan kesan memori. Model yang dicadangkan diterbitkan dari siri Volterra. Ia dibina dengan mengendalikan kesan memori lelurus dan taklelurus secara berasingan yang mana akan menyediakan pampasan herotan yang cekap dengan pelelurusan PA yang berkekompleksan rendah. Prestasi model yang dicadangkan dinilai menggunakan penguat kuasa kelas AB yang dikenakan dengan isyarat masukan jalur lebar dwi pembawa CDMA (WCDMA) dengan lebar jalur 15 MHz dan isyarat Evolusi Jangka Panjang (LTE) dengan labar jalur 15 MHz dan 20 MHz. Simulasi dan keputusan eksperimen menunjukkan bahawa model yang dicadangkan melebihi prestasi model MP dari segi prestasi nisbah kuasa kebocoran saluran bersebelahan (ACLR) masing-masing sebanyak 7 dB dan 6 dB bagi jalur lebar 15 MHz dan sebanyak 6.8 dB dan 6.5 dB bagi jalur lebar 20 MHz. Keputusan tersebut dicapai dengan pengurangan kekompleksan sebanyak 16% dari segi bilangan operasi titik-apung (FLOPs). Penyelidikan ini menunjukkan bahawa prestasi kelelurusan yang tinggi telah dicapai dan pada masa yang sama kekompleksan model DPD yang dicadangkan telah dikurangkan dengan ketara. Penambahbaikan ini akan

membawa kepada pengurangan kuasa dalam pemancar dan juga pengurangan sumber perkakasan yang diperlukan dalam pelaksanaan DPD atas cip.

ACKNOWLEDGEMENTS

I would like to express my deepest thanks and gratitude to my supervisor Assoc. Prof. Dr. Roslina Mohd. Sidek for her guidance, suggestions, and encouragement throughout this work. I have benefited from her deep knowledge and instructions on research. Without her support and help, this work would not been finished.

I would like to convey thanks and gratitude to my co-supervisor Dr. Nasri Bin Sulaiman for his support, guidance, and help. Also, I would like to thank my co-supervisor Dr. Pooria Varahram for his comments on this research.

I would like to extend my thanks to all the academic and administrative staff of Universiti Putra Malaysia for their help. Thanks and gratitude are extended to all my friends and colleagues for their support.

I am deeply grateful to my husband for his valuable help that he provided during my study. Also, I extend my deepest thanks and special appreciation to my daughters for their patience and support.

Finally, I would like to express my most affectionate thanks and gratitude to my mother for her unconditional love, encouragement, and great support throughout my whole life.

I certify that a Thesis Examination Committee has met on 17 June 2016 to conduct the final examination of Siba Monther Yousif on her thesis entitled "A Complexity-Reduced Digital Predistortion for Radio Frequency Power Amplifier" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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This is to confirm that:

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LIST OF ABBREVIATIONS

ACI	Adjacent Channel Interference
ACPR	Adjacent Channel Power Ratio
ACR-GMP	Augmented Complexity-Reduced Generalized Memory Polynomial
ACLR	Adjacent Channel Leakage Ratio
AM/AM	Amplitude Modulation to Amplitude Modulation
AM/PM	Amplitude Modulation to Phase Modulation
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CGC	Complex Gain Convergence
DPD	Digital Predistortion
DSP	Digital Signal Processing
EER	Envelope Elimination and Restoration
FOM	Figure Of Merit
EVM	Error Vector Magnitude
FLOPs	Floating point operations
FPGA	Field Programmable Gate Array
GMP	Generalized Memory Polynomial
IBO	Input Power Back Off
IF	Intermediate Frequency
IP3	Third-order Intercept Point
IMD	Inter Modulation Distortion
LINC	Linear amplification with Nonlinear Components
LTE	Long Term Evolution
LUT	Look Up Table
MP	Memory Polynomial
NMSE	Normalized Mean Square Error
OFDM	Orthogonal Frequency Division Multiplexing
OPBO	Output Power Back Off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratios
PH	Parallel Hammerstein
PLUME	Parallel-Look Up Table-Memory Polynomial-Enhanced Memory Polynomial

PSD	Power Spectral Density
PTNTB	Parallel Twin Non-linear Two-Box
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
VSA	Vector Signal Analyzer
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

CHAPTER 1

INTRODUCTION

1.1 Background

In wireless communication systems, transmitters are fundamental parts that have different specifications according to their applications, such as mobile and satellite systems. A generic transmitter is shown in Figure 1.1. It includes source and channel encoders, digital modulator, Digital/Analog (D/A) converter, Local Oscillator (LO), mixer, power amplifier, filters, and antenna.

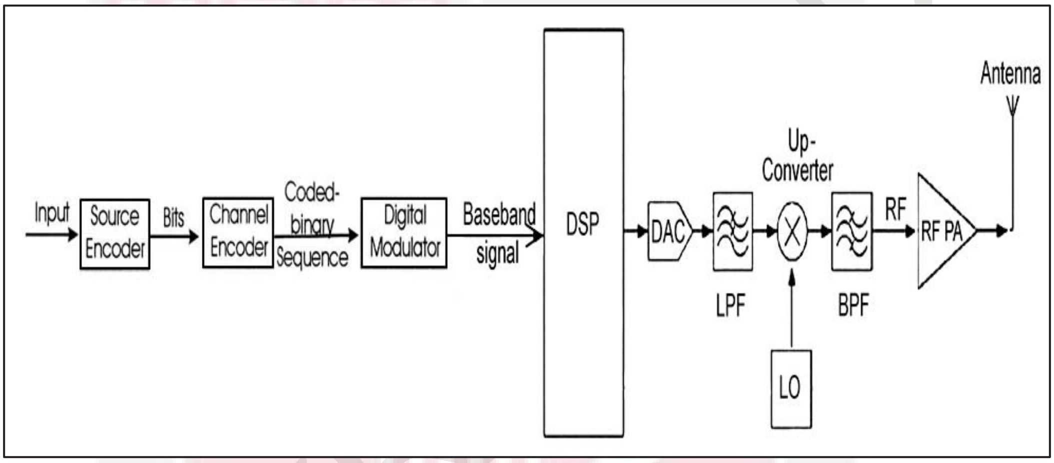

Figure 1.1: Block diagram of a transmitter

Initially, in Figure 1.1, the source encoder converts the input data to a stream of bits. The channel encoder codes these bits by introducing redundancy bits, which are used at the receiver, to combat the distortions due to the circuit nonlinearities, and the noise and interference introduced by the channel. Then, the digital modulator transforms the binary code sequence into signal waveform. This waveform, which is the baseband input signal, is manipulated using Digital Signal Processing (DSP) block. Then, the signal is converted to analog form and up-converted to RF frequency for transmission. The Power Amplifier (PA) is a very significant part in the transmitter and it is used to amplify the modulated signal in order to transmit it through the antenna. However, this PA is considered as one of the most power consuming parts in transmitters (Nuyts, Reynaert, & Dehaene, 2014).

In order to achieve high power-efficient Power Amplifiers (PAs), they are driven close to their saturation region. Consequently, these PAs are one of the main nonlinearity sources in transmitters. The nonlinearity contains out-of-band emission and in-band distortion. The former distortion causes adjacent channel interference (ACI) while the latter one reduces the bit error rate (BER) performance (Grebennikov, 2011). In modern high-speed wireless communications, increasing the demand of high spectral efficiency has resulted in the need to implement transmission formats, such as orthogonal frequency division multiplexing (OFDM) and code division multiple access (CDMA). However, these modulation schemes are more sensitive to the nonlinearities of power amplifiers because of their non-constant envelope signals (Fadhel M. Ghannouchi & Hammi, 2009). This issue can be solved by backing-off the operating region of the PA into a linear mode at the expense of power efficiency degradation of the PA. To solve this conflict between the power efficiency and the linearity of the power amplifier, a linearization technique is required (Gharaibeh, 2012).

Digital predistortion (DPD) is one of the most cost-effective linearization techniques, where linearization is achieved by predistorting the baseband signal, which is a standard modulated signal, before being applied to the PA. So, the DPD processing time is compatible with the source and channel encoders and is implemented as a nonlinear baseband component. This DPD represents the inverse of the nonlinearity behaviour of the PA. Therefore, by cascading these two nonlinearity subsystems, a linear system can be achieved (Farooq, Ishtiaq Ahmed, & Al, 2013), (Bu, Li, & Chen, 2014), and (Oualid Hammi, Zerguine, Hassan Abdelhafiz, & Ghannouchi, 2014).

1.2 Problem Statement

Modern communication signals, such as WiMAX, WCDMA, and LTE, have three parameters that might influence the behavior of PAs. These are the signal's average power, the signal's statistics (peak-to-average power ratio (PAPR) and probability density function), and the signal's bandwidth. Typically, the behavior of a PA is sensitive to variations in the operating average power with less than 1dB in some cases. Conversely, it is almost insensitive to the signal statistics (typically up to 3–4 dB variation in the signal's PAPR). Consequently, the different modulation levels do not affect the behavior of a PA as long as the signals' statistics follow the same distribution. On the other hand, the signal bandwidth has a direct impact on the memory effects exhibited by a PA and has a second-order effect on the static nonlinearity (Fadhel M. Ghannouchi & Hammi, 2009).

Therefore, as the bandwidth of the modern signal gets wider, PA begins to exhibit memory effects where PA output depends not only on the present input but also on the past input values (Y. Li, Zhu, Prikhodko, & Tkachenko, 2010), and (Kumagai, 2012). These memory effects result in a dynamic changing in the AM/AM and AM/PM characteristics of the PA. Hence, many complex schemes of DPD models have been introduced to accurately compensate the non-linearities with memory effects (Kumagai, 2012), and (You jiang Liu, Chen, Zhou, Zhou, & Ghannouchi, 2013).

However, high complexity predistorter algorithm leads to high power consumption (Tehrani et al., 2010). The complexity of DPD models includes number of coefficients used in the algorithms of these models and computational complexity when these models are utilized in real-time applications. Power consumption is a very important issue since PA is the most power consuming device in numerous applications, such as radio frequency transceivers (Jiwoo Kim, Roblin, Chaillot, & Xie, 2013) and wideband wireless communications (B. Gao, Xiao, Jin, Su, & Zhang, 2013). Therefore, designing low power consumption PA system while maintaining its performance is mostly required (Mohammady, Varahram, Sidek, Hamidon, & Sulaiman, 2010), (Sun, Yu, Liu, Li, & Li, 2014), and (Guan & Zhu, 2012).

Therefore, the main issue addressed by this thesis is the highly model complexity of the recent DPD designs, when enhancing the linearization capability of the DPD algorithms for PAs nonlinearity distortion. The nonlinearity distortion includes out-of-band emission, which causes adjacent channel interference and in-band distortion. Moreover, to achieve high data rate in 3G/4G applications, the memory effects of the PA must be considered in DPD modeling techniques. Therefore, the proposed design has addressed the memory effects of the PA as well.

1.3 Research Objectives

In this thesis, the main objectives are to:

1) Develope a digital predistortion model with low computational complexity in terms of number of floating operating points (FLOPs).
2) Enhance the PA linearity performance including out-of-band distortion in terms of Adjacent Channel Leakage Ratio (ACLR) and in-band distortion in terms of Error Vector Magnitude (EVM).
3) Compensate the linear and nonlinear memory effects, which cause the dynamic changes in the AM/AM and AM/PM of PA characteristics.

1.4 Scope of the Research

The scope of this research is shown in Figure 1.2, where the grey boxes show the flow direction of it. In this work, it was assumed that the power amplifier and the digital predistorter were the only nonlinear devices in the transmitter system in which all the nonlinearity distortion occurred from other electronic circuits, such as D/A converter and oscillator, are not considered. Moreover, only class-AB power amplifier was chosen to be tested in order to validate the linearization capability of the proposed predistorter since class-AB power amplifier can represent the current source amplifiers, which are A, B, and C classes. Meanwhile, the switches amplifiers, which are D, E, and F classes, are using different types of linearization techniques and therefore they are excluded from this research. The complex baseband input signals used were two-carrier WCDMA signal with 15-MHz bandwidth, which is generated from AWR software, and LTE signals of 15-MHz and 20-MHz bandwidth generated from Matlab. Furthermore, field measurement is not covered in this research.

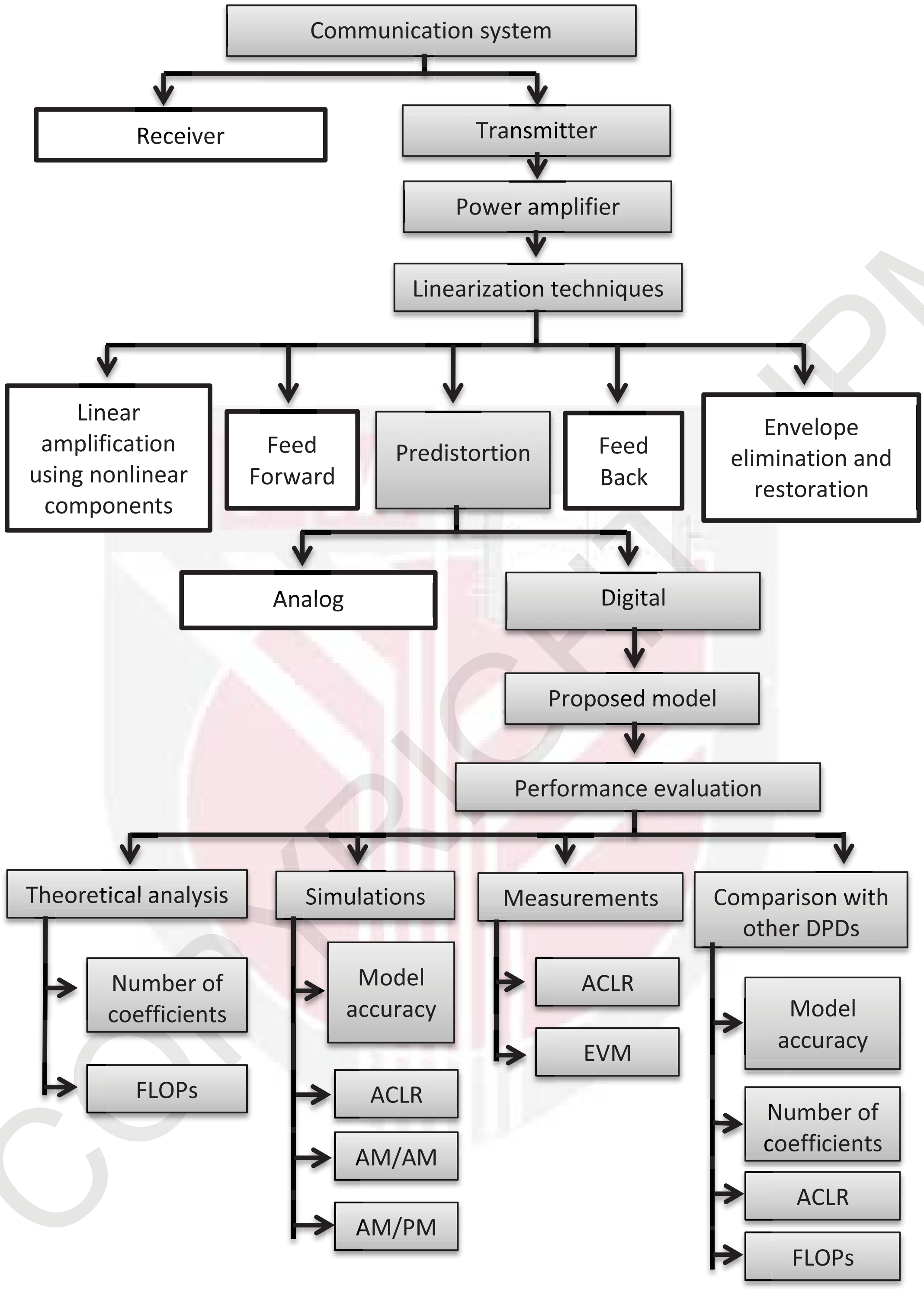

Figure 1.2: Block diagram of the research scope

1.5 Research Contribution

In this research, the contribution is to develope a low complexity DPD algorithm, which enhances the linearity performance of the PA with low computational cost consumed from the system. The PA linearity improvements include compensation of the spectral regrowth, which causes the adjacent channel interference, and the in-band distortion. Moreover, the proposed design addresses the PA memory effects, which cause dispersion of the signals utilized in modern wireless communication systems since these signals are wideband in order to gain high data rate.

Recent models have either limited linearity performance of PAs or high DPD computational complexity in practical applications. Therefore, it is essential to propose developed DPD models which reduce the model computational complexity and simultaneously achieve high linearization ability. Therefore, the proposed design consumes low running complexity and retains high linearization capabilities. This proposed design was verified using Matlab, validated using experimental measurements, and evaluated by comparing it with other models in terms of model complexity and linearity performance.

1.6 Thesis Organization

This research work concentrates on the topic of linearizing PAs using DPD technique, which is cost effective as well as maintains high overall efficiency of the system. The thesis is organized as follows:

Chapter 1 describes the problem statement, objectives, research methodology, and contribution of this work.

Chapter 2 presents the definitions of PA parameters and methods of amplification, while the trade-off between efficiency and linearity is revealed. Modeling PAs with and without memory effects is defined. An overview of the most existing linearization techniques including the feedback, feedforward, Linear Amplification using Nonlinear Components (LINC), Envelope Elimination and Restoration (EER), analog predistortion, and digital predistortion are introduced. The theoretical concept, main advantages, and drawbacks of each linearization technique are presented and discussed. The analysis of the model computational complexity is clarified in terms of FLOPs. The most commonly used digital predistortion methods with memory effects and the recent developments as well as the existing problems in the area of DPD linearization are highlighted.

In chapter 3, a low complexity digital predistortion model is proposed for linearizing PAs with memory effects. The derivative of the proposed design is demonstrated and the identification procedure for extracting the model coefficients is explained. Next, the proposed and MP models are analyzed to evaluate their model complexity in terms of number of FLOPs and number of coefficients used in each model. Next, the measurement set-up utilized in this work to validate the effectiveness of the proposed DPD is clarified. Then, the modeling process for the two PAs, proposed DPD, and MP predistorter are explained.

In chapter 4, the proposed predistorter for linearization of PAs with memory effects is verified using simulation environments. The simulation results based on linearity performance in terms of ACLR reduction are presented before and after applying the proposed and MP models. Moreover, dynamic AM/AM and AM/PM characteristics of PAs, before and after applying these predistorters, are illustrated to reveal the effectiveness of applying the proposed model as compared to the MP model.

In chapter 5, experimental measurements are performed to validate the effectiveness of the proposed predistorter. By using a real power amplifier driven by two input signals, the linearization capability of the proposed predistorter is evaluated and compared with the validity of the MP predistorter. This evaluation is based on the compensation of the in-band and out-of-band distortion in terms of EVM and ACLR performance, respectively. Moreover, a comparison is carried out between the simulation and experimental ACLR performance at the PA output after applying the proposed predistorter. Furthermore, a comparison is made between the proposed model and other works in terms of modeling accuracy, ACLR performance, number of FLOPs, and number of model coefficients.

Chapter 6 describes the conclusions of this research and suggestions for future work.

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