UNIVERSITI PUTRA MALAYSIA

DESIGN OF A WIDE-RANGE CMOS DIGITAL DELAY LINE WITH SUB-PICOSECOND JITTER FOR IMAGE SENSOR APPLICATIONS

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By

BILAL ISAM ABDULRAZZAQ

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Doctor of Philosophy

September 2016

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DEDICATION

To the memory of my mother and my beloved father for their love and endless support,

My beloved brothers (Sinan, Mustafa, and Anas), The Shoulders to Lean On

My lovely wife, My Soul Mate, for her patience and encouragement,

My beloved daughters (Lamees and Fatima), The Reasons to Get Through Another Day.

My Supervisor,

All my Supervisory Committee,

All of My Friends,

My beloved first and second country Iraq and Malaysia

"Without Your Support and Encouragement,

My Success Wouldn't Have Been Possible."

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the Degree of Doctor of Philosophy

DESIGN OF A WIDE-RANGE CMOS DIGITAL DELAY LINE WITH SUB-PICOSECOND JITTER FOR IMAGE SENSOR APPLICATIONS

By

BILAL ISAM ABDULRAZZAQ

September 2016

Chairman : Izhal Abdul Halin, PhD
Faculty : Engineering

Development of high-performance CMOS delay lines is becoming a crucial necessity for many advanced applications such as high-speed computer memory controllers and advanced time-resolved image sensors such as Time-of-Flight (ToF) image sensors and Fluorescence Lifetime Imaging Microscopy (FLIM) image sensors that would benefit from having a high-performance delay line integrated along with the system as a SoC solution. In this thesis, a 3-stage architecture CMOS digital delay line is proposed, designed, and analysed for generating picosecond-resolution delay steps, microsecond delay range, and at a sub-picosecond jitter performance.

To achieve wide delay range with fine-linear delay steps, a 3-stage circuit is proposed. In the first stage, a new 10-bit counter-based circuit is developed to allow a delay range of up to 2μs in steps of 2ns. The coarse delay output of this stage is fed to a medium-resolution second stage. The second stage uses a typical tapped-delay line topology that exploits the propagation delay of stacked logic circuits to generate medium-resolution delay steps. This stage generates a delay range of 2ns with steps of 65ps. This stage is used to interpolate between the coarse-resolution delay steps generated in the first stage. The output of this stage is then fed to a third stage designed using a Delay-Locked Loop (DLL) circuit with a new charge resetting technique. The charge pump of the DLL is reset by a specialized circuit designed to trigger using the input signal that is to be delayed. A small-signal model of the proposed circuit along with analytical modeling are presented to show the relationship between the DLL's internal control voltage and output fine time delay steps. The delay range generated for this last and third stage is 70ps with a step of 1ps. This fine delay stage is used to interpolate between the medium-resolution delay steps generated in the second stage. The output of the entire delay line is read at the output of this final stage.

The delay specifications for the 3-stage CMOS digital delay line in this work are confirmed by simulation using a standard 0.13μm Silterra CMOS process. Apart from the mentioned delay specifications, analyses show that the Integral-Non Linearity (INL) of the first stage, second stage, and third stage is 0.13LSB, 1.94LSB, and 1.7LSB, respectively. The jitter performance at the output of the third stage is only 0.39ps RMS. The total power consumption of the full implemented 3-stage CMOS digital delay line circuit is only 2.7 μW. The active layout area of this delay line is approximately (285×220) μm^2 making it suitable to be integrated as a SoC solution for chips that may require high-delay specifications.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk Ijazah Doktor Falsafah

REKABENTUK TALIAN LAMBATAN CMOS BERJARAK JAUH DENGAN KETARAN WAKTU SUB-PIKO SAAT UNTUK PENGAPLIKASI SENSOR IMEJ

Oleh

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Keperluan talian lambatan masa berprestasi tinggi menjadi semakin penting untuk aplikasi termaju seperti pengawal memori komputer berkelajuan tinggi dan penderia imej kawalan masa termaju seperti penderia imej masa penerbangan dan penderia imej jangkahayat fluorescene di mana sistem-sistem ini mendapat manfaat besar apabila diintegrasi dengan talian lambatan masa tersebut dalam sesebuah penyelesaian SoC. Dalam tesis ini, sebuah talian lambatan masa CMOS 3-tahap dicadangkan, direkabentuk dan dianalisa untuk menghasilkan langkah lambatan masa piko-saat, jarak lambatan masa mikro-saat dengan kejituan masa sub-piko-saat.

Rekabentuk 3-tahap dicadangkan untuk menghasilkan jarak lambatan masa panjang dengan langkah lambatan masa halus. Tahap pertama menonjolkan rekabantuk litar baru yang berdasarkan litar pembilang digit 10-bit untuk menghasilkan jarak lambatan 2μs dengan langkah lambatan 2ns. Keluaran lambatan masa yang kasar di tahap ini digunakan sebagai masukan untuk tahap kedua yang lebih halus lambatan masanya. Tahap kedua pula menggunakan topologi litar biasa di mana lengah perambatan litar-litar lojik digunakan untuk menghasilkan lambatan masa beresolusi separa halus. Tahap kedua ini menghasilakn jarak lambatan 2ns dengan langkah lambatan 65ps. Keluaran tahap ini digunakan untuk menginterpolasi langkah lambatan masa kasar yang dihasilkan oleh tahap pertama. Keluaran tahap kedua ini pula digunakan sebagai masukan untuk tahap ketiga yang direkabentuk menggunakan sebuah DLL yang beroperasi dengan baru yang diperkenalkan iaitu kaedah set-semula cas. Pam cas DLL tersebut disambungkan kepada sebuah litar penyahcas baru yang digera menggunakan isyarat masukan yang hendak dilambatkan. Sebuah model isyarat kecil litar tersebut dan analisis matematiknya dipersembahkan untuk menunjukkan hubungan di antara voltan kawalan dalaman DLL tersebut dengan keluaran langkah lambatan masa halus yang terhasil. Jarak lambatan yang dihasilkan oleh tahap ini adalah 70ps dengan langkah 1ps. Langkah lambatan masa halus ini digunakan untuk menginterpolasi antara masa langkah

lambatan yang dihasilkan oleh tahap kedua yang separa halus. Keluaran litar lambatan keseluruhan diperolehi dari keluaran tahap ketiga ini.

Spesifikasi lambatan masa untuk litar 3-tahap ini disahkan dengan simulasi litar proses CMOS Silterra 0.13μm. Selain dari spesifikasi lambatan masa, analisa data simulasi menunjukkan INL untuk tahap pertama, kedua dan ketiga adalah masing-masing 0.13LSB, 1.94LSB, dan 1.7LSB. Prestasi ketaran untuk tahap ketiga pula memberi kejituan yang bernilai 0.39ps RMS. Penggunaan kuasa keseluruhan pula hanyalah 2.7 μW. Luas kawasan aktif litar keseluruhannya pula hanyalah (285 220) μm^2 menjadikan litar ini sesuai diintegrasi dalam mana-mana chip sebagai penyelesaian SoC yang memerlukan spesifikasi lambatan masa setinggi ini.

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I certify that a Thesis Examination Committee has met on 9 September 2016 to conduct the final examination of Bilal Isam Abdulrazzaq on his thesis entitled "Design of a Wide-Range CMOS Digital Delay Line with Sub-Picosecond Jitter for Image Sensor Applications" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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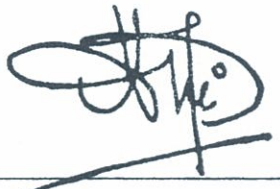

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BCD	Binary-Coded-Decimal
BJT	Bipolar Junction Transistor
BPTM	Berkeley Predictive Technology Model
CDR	Clock-Data Recovery
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CMP	Comparator
CP	Charge Pump
CRC	Capacitor-Reset Circuit
CRDL	Coarse-Resolution Delay Line
CSI	Current-Starved Inverter
DA	Design Architect
DAC	Digital-to-Analog Converter
DCD	Duty-Cycle Distortion
DCDL	Digitally-Controlled Delay Line
DDC	Differential Delay Cell
DLL	Delay-Locked Loop
DNL	Differential-Non-Linearity
DR	Delay Range
DS	Delay Step
DSM	Deep Sub-Micron
DTC	Digital-to-Time Converter
EMI	Electromagnetic Interference

FF	Fast-Fast process corner
FRDL	Fine-Resolution Delay Line
FS	Fast-Slow
FSM	Finite-State Machine
G.CLK	Gated clock
HCI	Hot-Carrier Injection
IC	Integrated Circuit
IIPDPT	Interfoundry Inverter Propagation Delay with Process Technology
INL	Integral-Non-Linearity
LF	Loop Filter
LSB	Least-Significant Bit
MRDL	Medium-Resolution Delay Line
NBTI	Negative Bias Temperature Instability
nMOS	negative Metal Oxide Semiconductor
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
pMOS	positive Metal Oxide Semiconductor
P-P	Peak-to-Peak
PS	Phase Selector
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage, and Temperature
RMS	Root-Mean Square
RST	Reset
SCI	Shunt-Capacitor Inverter

SF	Slow-Fast process corner
SoC	System-on-Chip
SR	Set-Reset flip flop
SS	Slow-Slow process corner
std	Standard deviation
TDC	Time-to-Digital Converter
TDDB	Time-Dependent Dielectric Breakdown
TDL	Tapped-Delay Line
TIM	Time-Interval Measurement
ToF	Time-of-Flight
TT	Typical-Typical process corner
UDSM	Ultra-Deep Sub-Micron
VCDL	Voltage-Controlled Delay Line
VCO	Voltage-Controlled Oscillator
VDL	Vernier-Delay Line
VLSI	Very-Large Scale Integration

LIST OF SYMBOLS

L	Transistor channel length
W	Transistor channel width
C_L	Load capacitance
V_{DD}	Supply voltage
μ	Carrier mobility
C_{ox}	Gate-oxide capacitance
V_{TH}	Threshold voltage
α	Technology parameter used to express the carrier-velocity saturation effect
I_0	Initial value of the controlling current
ΔI	Change in controlling current
τ_D	Time delay
$\Delta\tau_D$	Change in time delay
V_{bp}	pMOS bias voltage
v_c	Control voltage
t_T	Input waveform transition time
I_D	Drain current
V_{GS}	Gate-to-source voltage
T_{ox}	Gate-oxide thickness
ε_{ox}	Oxide permittivity
I_{Dsat}	Drain saturation current
μ_n	Carrier mobility for nMOS electrons
μ_p	Carrier mobility for pMOS holes
$\sigma^2_{T_{pd}}$	Variance of propagation delay

R_w	Interconnect resistance
T	Time constant
ρ	Resistivity
w	Width of the interconnect
t	Thickness of the interconnect
l	Length of the interconnect
$V_{thermal,rms}$	RMS voltage of the thermal noise
K_B	Boltzmann constant
T	Absolute temperature
Δf	Bandwidth
T_u	Absolute resolution
$t_{d,n}$	Time delay of the *n*th delay element
ε	Delay error
$t'_{d,n}$	Delay step position
$S_{V_{DD}}^{\tau_D}$	Delay sensitivity to supply voltage fluctuations
ΔV_{DD}	Supply voltage variation
T_r	Room temperature
$t_{d,N}$	Time delay at the end of the CMOS delay line
η	Delay shift induced by noise error
ΔT_{abs}	Absolute/long-term jitter
ΔT_c	Cycle jitter
$\Delta T_{c\text{-}c}$	Cycle-to-cycle jitter
$D_{VCDL(min)}$	Minimum VCDL delay
$D_{VCDL(max)}$	Maximum VCDL delay

T_{ref}	Period of the input reference signal
$\sigma\left(\Delta d_{VCDL}^{2}\right)$	Total timing error variance of the total VCDL
$\sigma(\Delta d^{2})$	Timing error variance of the unit delay element
I_{CP}	Charge pump current
K_d	Delay element gain
C_f	Capacitance of the loop filter's capacitor
ϕ_{offset}	Undesired phase shift
Δt_{on}	Pulse-width of the UP or DOWN pulse from the phase detector
Δi	Current mismatch
T_C	Cycle period
P_{IN}	Input signal to the Trigger Generator circuit
P_D	Output delayed signal from the Delay Generator circuit
T_{dC}	Coarse time delay
T_W	Pulse width of the output delayed signal
P_{OUT1}	Output signal from CRDL stage
$P_{OUT1,int}$	Output signal from CRDL stage delayed by the intrinsic delay of the CRDL's building blocks
$P_{OUT1,min}$	Output signal from CRDL stage delayed by the minimum coarse delay step
$P_{OUT1,max}$	Output signal from CRDL stage delayed by the maximum coarse delay range
TRG_P’	Output signal from Trigger Generator circuit
STOP_P_D	Stop pulse of the Delay Generator circuit
$DS_{C,min}$	Minimum coarse delay step
$DR_{C,max}$	Maximum coarse delay range
f_{clock}	Frequency of the counter clock

$2^{counter,bits-no.}$	2 powered to the counter bit-number
STOP_P_D	Stop pulse of the Duty-Cycle Controller circuit
$T_{W,max}$	Maximum pulse width of the output delayed signal
$DS_{M,min}$	Minimum medium delay step
P_{OUT2}	Output signal from MRDL stage
$P_{OUT2,min}$	Output signal from MRDL stage delayed by the minimum medium delay step
$P_{OUT2,max}$	Output signal from MRDL stage delayed by the maximum medium delay range
$DR_{M,max}$	Maximum medium delay range
N	Number of delay stages
$DS_{F,min}$	Minimum fine delay step
$DR_{F,max}$	Maximum fine delay range
P_{OUT}	Output signal from FRDL stage
$P_{OUT,nom}$	Output signal from FRDL stage delayed by the nominal delay of the DLL
$P_{OUT,min}$	Output signal from FRDL stage delayed by the minimum fine delay step
$P_{OUT,max}$	Output signal from FRDL stage delayed by the maximum fine delay range
ϕ_R	Reset pulse
τ_R	Time constant of the loop filter
v_0	Initial voltage across the loop filter's capacitor
g_m	Transistor transconductance
r_{ds}	Drain-to-source resistance
Δg_m	Change in transconductance

Δr_{ds}	Change in drain-to-source resistance
T_{dM}	Medium time delay
T_{dF}	Fine time delay
K_{VCDL}	Gain of the VCDL
Δd_{VCDL}	Jitter caused by the VCDL
Δd_{dC}	Jitter generated from the CRDL stage
Δd_{dM}	Jitter generated from the MRDL stage
Δd_{dF}	Jitter generated from the FRDL stage
ΔR	Change in the resistance
Δt	Difference between different discharging times
$T_{discharge,min}$	Minimum discharging time
$T_{discharge,max}$	Maximum discharging time
$t_{charge,min}$	Minimum charging time
$t_{charge,max}$	Maximum charging time
$T_{d,tot}$	Total time delay

CHAPTER 1

INTRODUCTION

This chapter presents an introduction of the work carried out. A background on time management circuits is first presented with a focus on the importance of these circuits in science and industry applications. Then, a section on the limitations of conventional CMOS delay lines is presented, which explains how the problem statements have been formed as a result of the drawbacks found in the contemporary available CMOS delay lines. Subsequently, the research problem statements are listed in detail before presenting the research aim and objectives. To conclude this chapter, the research scope is discussed, followed by the thesis organization.

1.1 Research background

Time delay circuits, sometimes called time management circuits, serve the purpose of controlling the time difference between clocks or other pulses by adding/eliminating a pre-specified time delay. Moreover, depending on their application, these circuits can also be designed to control the duty cycle of an input pulse [1]. Time delay circuits are characterized by their delay range, delay step, and jitter performance. The delay range is the maximum time a signal can be delayed, while the delay step is a measure of the finest incremental time step a time delay circuit can produce. On the other hand, jitter is the time uncertainty in an output delayed signal and directly affects the smallest delay step [2-4].

There are two types of delay lines summarized in Figure 1.1. The first type shown in Figure 1.1 (a) delays a true input signal by an amount τ_D. The value of τ_D can be programmed by a digital word. The second type of delay lines is shown in Figure 1.1 (b). This type uses an input trigger pulse and a Trigger Generator (TG) circuit to generate an output delayed signal. The output time delay is measured from the rising edge of the input trigger pulse to the rising edge of the output pulse. PW is used to control the pulse width of the output delayed pulse [1,5].

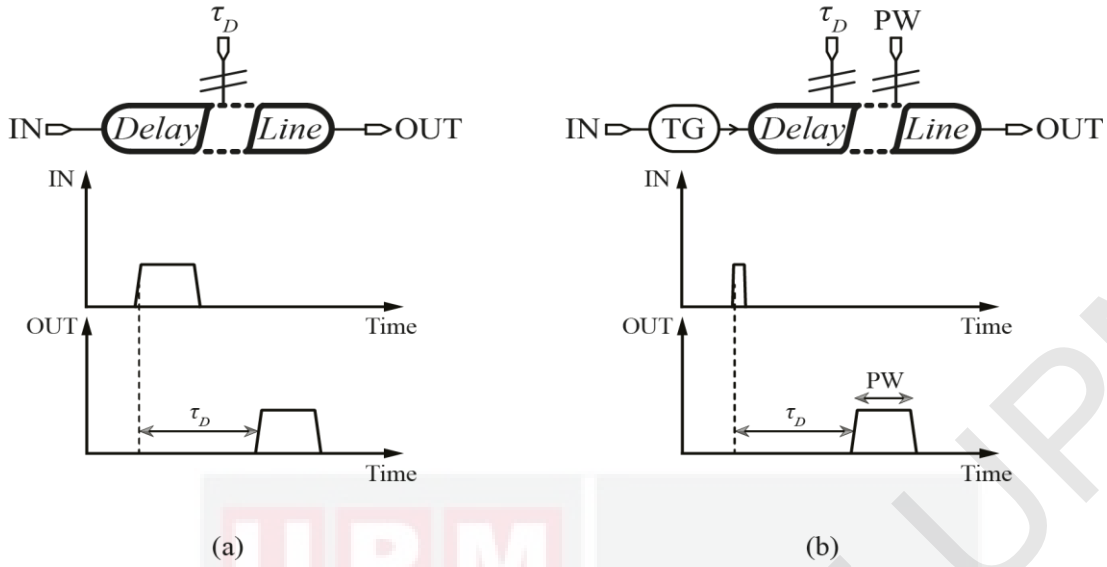

Figure 1.1 : Programmable delay lines (a) with a true input signal. (b) with a trigger reference pulse.

In this work, the second type of delay lines shown in Figure 1.1 (b) is studied for application in a Fluorescence Lifetime Imaging Microscopy (FLIM) image sensor.

FLIM CMOS image sensors are used to capture biological cell images without the use of staining chemicals. They work by illuminating a short light pulse on the cell which will in turn produce bio-fluorescence light that is captured by pixels of the sensor. Since this bio-fluoroscec light decays exponentially over a period of 1µs, the pixel exposure time window is synchronized with the light pulse source and moved in fine-resolution delay increments over a delay range of 1µs, enabling many images related to sections of the decaying light samples to be obtained by the pixel for image construction. Currently, the experimental setup for imaging uses an external CMOS digital delay line for shifting the imaging window. However, it is desirable to integrate the delay line as a part of the image sensor system that can easily be packaged as a compact camera [6].

Time-of-Flight (ToF) range image sensors acquire range images of a scene by using a ToF light source synchronized with the imagers capture window. They work by measuring the time-of-flight a light signal, emitted from the ToF light that is in-line with the ToF sensor, takes to travel to and from objects in a scene back to the sensor. In quantifying ToF sensors, delay lines are used to vary the delay of a ToF light source that back-reflects the light signal on a fixed white surface. Delay lines are used to delay the ToF light source in order to mimic objects at different distances even though a white fixed board is used. This technique considerably simplifies the measurement setup and process [7,8]. As ToF sensors are constantly evolving to measure micrometric-resolution distance within metric-range distance [9], delay lines should also be redesigned for picosecond and microsecond-range delays.

CMOS delay lines are also used in on-chip time measurements and the synchronization of a CPU with its interfaces [10,11]. To illustrate the synchronization application of the delay lines, Figure 1.2 is presented which shows the location of the delay line circuit.

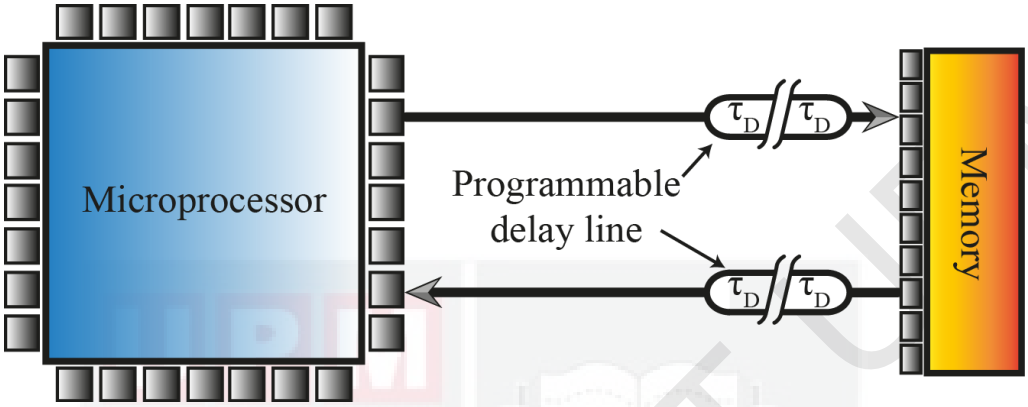

Figure 1.2 : Application of a delay line as a synchronization circuit.

In Figure 1.2, the function of the programmable delay line is to ensure perfect synchronization of data packets at both the transmitting and receiving ends. This is to avoid functionality failure of the system. Since CMOS technology scaling and clock speeds are continuously progressing, chip size becomes smaller and the synchronization process becomes more challenging. Accordingly, design of a single- circuit block delay line, which can be integrated with the computer memory interface, becomes a necessity.

1.2 Limitations of CMOS Delay Lines

There are two main issues with conventional CMOS delay lines. The first issue is the jitter performance which is in the range of several picoseconds [12,13]. As jitter performance directly affects the finest achievable delay resolution, it is considered a crucial factor in determining the performance of delay lines [4]. Although the jitter performance of CMOS delay lines is not as fine as that of optics-based delay lines, extensive work to produce sub-picosecond jitter performance CMOS delay lines is actively undertaken by many parties due to the fact that IC-based delay lines are robust in terms of system integration and cost reduction when compared to their optical counterpart. The second issue is in realizing a delay line that has an exceptionally long delay range with fine, uniform, and linear delay steps [13]. Fine-resolution solid-state circuit delay lines cannot simply be cascaded like optical delay lines because delay increments are non-linear mainly due to the complex nature of the parasitic capacitance network in the delay elements of the delay line [14]. The cascading methodology also leads to a complex PCB implementation. Thus, a single chip solution should be developed to overcome these shortcomings.

1.3 Problem statements

As CMOS technology continuously evolves and the operating frequency of Integrated Circuits (ICs) constantly increases, achieving precise time managements becomes more challenging. This is due first to the reduced timing margins between signals within ICs and second to the significantly increasing effects of the Process, supply Voltage, and Temperature (PVT) variations. The increase in operating frequencies as CMOS technology scales down causes delay resolution to degrade because of the increase in timing jitter. Although significant improvements have been realized in terms of obtaining either wide delay range such as 46ns [15] and 160ns [16], high-resolution delay steps such as 2ps [15] and 0.5ps [17], or remarkable jitter performance such as 0.1ps RMS [18] and 0.03ps RMS [19], these improvements may not satisfy the growing needs of today's and future's SoC applications. This is attributed to the fact that SoC applications, such as high-speed computer memories [20], on-chip time measurements [18] and time-dependent image sensors [6], require all the aforementioned high-delay specifications to be integrated together in one single-circuit block [13].

Through literature review presented in Chapter 2, it is concluded that there is a trade-off between delay range and delay resolution. The longer the maximum delay allowed by a circuit, the larger the steps are. For FLIM imaging applications, this is not desirable. Therefore, there is a necessity to realize a circuit that embodies both wide delay range and high-resolution delay steps.

1.4 Research aim and objectives

This work aims to develop a CMOS delay line that minimizes the trade-off between wide delay range and high-resolution delay steps. The delay line will function according to Figure 1.1 (b) where the time delay is measured with respect to the rising edge of a trigger pulse and the output delayed signal, whose pulse width can be varied. Since this delay line is to be integrated with a FLIM image sensor, the targeted delay range is 2µs with a 1ps delay step. The jitter performance should be no more than 0.5ps RMS. Towards the achievement of the proposed research goals, the following objectives are to be carried out:

1. To investigate the circuit techniques used for obtaining both wide delay range and fine delay steps. For this, a study on the number of delay stages utilized in previous CMOS delay lines for the sake of increasing the maximum achievable delay range to the microsecond range is to be carried out.

2. To investigate circuit techniques for designing a coarse-resolution delay step circuit with long delay range that is not power hungry.

3. To investigate the circuit techniques targeted for achieving fine-resolution delay steps. This is for refining the finest achievable delay step to picosecond-resolution linear steps within a fine delay range of several tens of picosecond-linear steps.

4. To investigate minimization of Delay-Locked Loop's output jitter to sub-picosecond for a fine delay range of several tens of picoseconds. This specific amount of the output jitter is set in order not to deteriorate the picosecond-resolution delay steps.

1.5 Research scope

To achieve the goals of this work, a 3-stage delay line topology is proposed. The idea behind this is that different stages will produce different delay range and different delay step sizes and when combined, a long-range fine-step delay line is produced. The proposed microsecond-range picosecond-step delay line is targeted for the application in FLIM image sensor whose fluorescence light's lifetime is in the microsecond range.

As a summary, the first stage is designed to produce the pulse width of the output delayed pulse as well as introduce a long delay range with coarse-uniform delay steps. The output of this stage is fed to the second stage which fine tunes the delay to medium-resolution steps. The output from the second stage serves as input to the final stage that is responsible to further fine tune the delay steps into the picosecond value and at the same time minimize jitter.

The scope of this research is limited to circuit design through analytical modeling and the use of industrial standard methodology of computer post-layout simulation for verification of the performance parameters set in the goal of this thesis. The CMOS technology used in the design of the proposed work is 0.13µm Silterra.

1.6 Thesis organization

This thesis is structured into five chapters. Chapter 1 presents an overview of the research area, focusing on the problems of the contemporary available delay line architectures that motivated this work. In addition, this chapter demonstrates the problem statements, aim, objectives, and scope of the research. Chapter 2 presents a comprehensive review on the existing CMOS delay line architectures, topologies, and control techniques. The effects of CMOS technology scaling, PVT variations, and noise sources as well as jitter on CMOS delay lines are also discussed. The use of DLLs and Phase-Locked Loops (PLLs) as high-resolution delay lines is also included and the difference between them is also discussed. The most relevant reported works to this work are critically reviewed, showing the trade-off in the performance of these works. The chapter ends with highlighting the main issues that should be taken into consideration when designing a CMOS delay line circuit with high-delay specifications.

Chapter 3 gives the full description of the research methodology. The circuit designed for this work is divided into three stages. As mentioned previously, the first stage uses a novel circuit that is responsible for the generation of the maximum

delay range with coarse and uniform steps. In this stage, an input trigger pulse creates an output signal whose duty cycle and delay with respect to the trigger pulse can be programmed. The second stage interpolates the minimum-coarse delay step of the first stage. The last stage is responsible for generating the finest-resolution delay step and maintaining the output jitter in the sub-picosecond range. Detailed explanation using small-signal model is presented for better comprehension of how fine delay steps are achieved using the proprietary charge pump circuit. Analytical equations are derived to show the relationship between the proposed circuit's small-signal model control voltage and generated fine delay steps.

Chapter 4 presents the post-layout simulation results. Analysis including non-linearity, PVT variations, and jitter is also presented and discussed.

The thesis is ended with Chapter 5 that summarizes, concludes, and presents a list of contributions of this work. Potential ideas to be pursued as future works are also suggested.

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