

Implementation of multi-class shared buffer with finite memory size

ABSTRACT

High packet network have become an essential in modern multimedia communication. Shared buffer is commonly used to utilize the buffer in the switch. In this paper, we analyse the performance of shared buffer with different memory sizes. The architecture of the multi-class shared buffer is developed for 16×16 ports switch that is targeted in Xilinx FPGA. The performance of the multi-class shared buffer switch is analysed in term of throughput and mean delay. Based on the simulation with different memory sizes, it is observed that the optimum selection of memory size under uniform traffic depends on the maximum traffic load of the switch.

Keyword: Shared buffer; Multi-class; Finite memory size; Architecture design; FPGA