Impact of intrinsic parameter fluctuation on the fault tolerance of L1 data cache

ABSTRACT

As the semiconductor process technology continues to scale deeper into the nanometer region, the intrinsic parameter fluctuations will aggressively affect the performance and reliability of future microprocessors and System-on-Chip (SoC) applications. These system requires large SRAM arrays that occupy an increasing fraction of the chip real estate. To investigate the impact various source of intrinsic parameter fluctuation (IPF) from systems point of view, a framework to bridge architecture-level and device-level simulation will be utilized for data cache built from transistors with 25 nm, 18 nm and 13 nm technology node. This study found that the IPF will not have any significant impacts on data cache memory systems build with 25 nm while increasing the memory cell ratio, (ß) to two will overcome the IPF impacts for the 18 nm. However, the 13 nm technology data cache could not operate even with higher cell ratio. Common, cache memory fault detection and correction such as ECC and redundancy can only partially remove the transaction error caused by these fluctuation sources.