DSP implementation of digital pre-distortion in wireless communication systems

ABSTRACT

This paper presents a Digital Signal Processor (DSP) implementation of Digital Pre-distortion (DPD) targeting the 3rd Generation/4th Generation (3G/4G) wireless networks. The non-linearity of the Power Amplifier (PA) causes several issues such as Adjacent Channel Interference (ACI), power wastage, high energy consumption, and system inefficiency. These shortcomings result in performance limitation for the wireless communications system which is undesirable for the industry. DPD is chosen as the PA linearization method due to its overall advantages in Adjacent Channel Power Reduction (ACPR), cost, efficiency, and implementation flexibility. The DPD system is developed using the C++ Hardware Programming Language in order to be implemented into the target Digital Signal Processor (DSP), the soft-core Microblaze processor by Xilinx. The developed system in C++ is compared with the conventional Matlab Simulation and a performance difference of 0-10dB in ACPR is observed. The C++ DSP Implementation is capable of achieving up to 15dB of ACPR for WiMAX signal in 4G networks and 25dB for 2-carrier Wideband Code Division Multiple Access (2C-WCDMA) signals in 3G networks.

Keyword: Power amplifier; PA linearization; Digital pre-distortion; MATLAB; C++; 3G; 4G