

Power - reliability tradeoff in low power 4-PAM signaling in on-chip communication

ABSTRACT

The higher data rates at low power consumption have recently directed attentions towards on/off-chip multilevel signaling. However, its tighter noise margin cost leads to reliability concern. In this work, the reliability issue for multilevel signaling is highlighted using 4-PAM scheme. Three cost-effective architectures based on Hamming codes are synthesized in 45-nm technology to analyze the tradeoffs between reliability improvement and power consumption. Results showed that the 8-(7,4) configuration can enhance the 4-PAM signaling performance more than 3.3-dB at the Bit Error Rate of 10^{-6} while reducing power consumption up to 58% against binary for a 10-mm global on-chip interconnect. Furthermore, it is shown that higher levels of reliability are achievable at the cost of lower power savings. This paper provides guidelines to the designers for selecting between signaling schemes given the design characteristics and constraints.

Keyword: Multilevel signaling; Forward error correction; Low power on-chip communication; Fault tolerant technique