A new cascaded multilevel inverter topology with minimum number of conducting switches

ABSTRACT

There are many advantages of the cascaded multilevel inverter such as low voltage stress for each switching device and higher power quality. The main drawback for this type of inverter is the high number of switching device it needs in an installation. In order to reduce total harmonics distortion (THD) of the output voltage waveform, the number of output voltage level need to be increased, hence the higher number of switching devices. This subsequently increases the installation cost, inverter circuit size and power losses - in the form of heat and voltage losses in the inverter circuit. In this paper a new cascaded multilevel inverter topology is proposed with a minimum number of switching devices and driver circuits needed. The proposed new topology also needs to turn on only three switching devices at any operation time for any output voltage level configurations. The new cascaded multilevel inverter topology validity is verified by the simulation and experimental results of a prototype single phase 41-level inverter. The prototype inverter can also be designed to supply a load with a specific power factor requirement.

Keyword: Multilevel inverter; Reduced switching devices; Minimum conducting switches; MOSFET; Low THD