**A simulation study of thickness effect in performance of double lateral gate junctionless transistors**


ABSTRACT

The electrical behaviour of double lateral gate junctionless transistors, regarding to the variation of channel thickness is investigated, through 3-D numerical simulations. The simulation results explicitly show that how the device thickness affect the on and off current and threshold voltage behavior based on variation of the carriers density and recombination rates of the carriers. As the channel thickness is decreased, the amount of bulk neutral channel getting smaller which cause a decrease in the on state current. Meanwhile, the lateral gate influence on the channel is reinforced, which cause a decrease in leakage current in the off state. Threshold voltage is decreased as the channel thickness decreases. However, the recombination rate of carriers increases with decreasing the channel thickness, due to the accumulation of minority carries and shifted to the source side of the channel.



**Keyword:** Junctionless transistor; Lateral gate; Thickness effect; TCAD simulation