Numerical investigation of channel width variation in junctionless transistors performance

ABSTRACT

Double gate junctionless (DGJLT) transistor, as a pinch off device, was previously fabricated. In this letter, the impact of channel width variation on behaviour of the device is studied by means of 3D-TCAD simulation tool. In this matter, the transfer characteristics, energy band diagram (valence/conduction band) and normal electric field along the nanowire between the source and the drain are studied at pinch off state. By decreasing the nanowire width, the on current decreases. Threshold voltage also reduced by decreasing the wire width. The highest electric field occurs at off state and the normal component of the electric field is stronger for smaller channel width. At pinch off state, the energy band diagrams revealed that a potential barrier against the current flow was built in channel which the smallest width has higher potential barrier. The overall result agrees with the behaviour of the nanowire junctionless transistors.

Keyword: Lateral gate junctionless transistor; Energy band diagram; Channel width effect; TCAD simulation