Design of 8-bit SAR-ADC CMOS

ABSTRACT

Successive approximation analog-to-digital converter (ADC) implemented in a conventional 0.18εm CMOS technology with low voltage. The SAR composite of sample-and-hold dummy switch compensation was employed, comparator is low-voltage latched and realized based on current-mode approach, control logic circuit and digital-to-analog conversion consists of binary weighted capacitor arrays for the differential inputs. The ADC has INL and DNL of 0.45 LSB for supply voltage 1.8V, at sampling rate 200 KS/S and signal to noise ratio distortion is 58.5 dB. This design is suitable for standard CMOS technology with low-power low-cost VLSI implementation. It is well applied when embedded into system-on-chip (SOC) circuit designs.

Keyword: Analog-to-digital converter; CMOS; Comparator; Digital-to-analog converter; Low voltage; Sample-and-hold