Interconnect area, delay and area-delay optimization for multi-level signaling on-chip bus

ABSTRACT

In this paper, the technique of optimal interconnects width and spacing is analyzed to reduce the area, delay and area-delay-product of multi-level signaling on-chip bus. To capture the delay impact from cross-coupling capacitance in the deep sub-micron on-chip bus, the Miller Capacitance Factor (MCF) for 4-level signals is developed. Results show that our proposed technique reveals the trade-off between bus area and delay to achieve the optimized bus configuration.

Keyword: Multilevel signaling; Interconnect delay; Interconnect optimization; Coupling capacitance