

A process variation aware system-level framework to model on-chip communication system in support of fault tolerant analysis

ABSTRACT

On-chip interconnect communication system consists of the drivers, interconnect wires and receivers. Several on-chip communication system models have been developed for the purpose of on-chip fault-tolerant communication research. While most of these models improved the channel modeling, the effects of the drivers and receivers to the whole communication system were largely ignored. In this paper, we introduce a comprehensive, system-level framework, to capture and integrate the characteristics of the channel as well as the drivers and receivers. The proposed framework offers a methodology to model the on-chip interconnect communication system and can provide a flexible and updateable platform to evaluate fault-tolerant communication approaches. Furthermore, the current deterministic paradigm which end is worst case analysis pessimism is avoided by shifting towards statistical design flow to reduce uncertainties caused by process variation.

Keyword: On-chip communication; Process variation; Fault tolerant analysis; System-level modeling; Deep submicron (DSM)