

FPGA implementation of the proposed DSI-SLM scheme for PAPR reduction in OFDM systems

ABSTRACT

High peak to average power ratio (PAPR) is the main drawback of orthogonal frequency division multiplexing (OFDM) systems. Some of the proposed PAPR reduction solutions are dummy insertion (DSI), selected mapping (SLM) and combined DSI-SLM scheme. This paper presents FPGA implementation of DSI-SLM scheme for OFDM signals. The results of the implementation and simulation are compared which show that the PAPR is almost the same as simulation results. The hardware resource consumption of the DSI-SLM method is estimated to be at least 4 times less than conventional SLM (C-SLM) method with comparable PAPR performance.

Keyword: C-SLM; DSI; Hardware consumption; IFFT; Transmission efficiency; WiMAX