An FPGA implementation and performance analysis between radix-2 and radix-4 of 4096 point FFT

ABSTRACT

The rapid grown in wireless 4G and 5G technology push to the edge to high input data processing. High input data processing required advance Orthogonal Frequency Division Multiplexing (OFDM). The main block in any OFDM transceiver is the Fast Fourier Transform (FFT). FFT consider the transformation bridge between the time and frequency domains. In this research an implementation and direct analysis between radix-2 and radix-4 FFT algorithms presented. Memory-based architecture adopted for the all algorithms. The entire algorithm designed by Altera Quartus II and synthesis for Altera DE2-70 field programmable gate arrays (FPGA) board, in order to investigate and determine the desired algorithm based on the application used for and the system requirement.

Keyword: FFT; Radix-2; Radix-4; FPGA; Memory-based architecture