UNIVERSITI PUTRA MALAYSIA

SIGMA-DELTA ANALOG TO DIGITAL CONVERTER ON FIELD PROGRAMMABLE GATE ARRAY

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Master of Science

February 2015

DEDICATION
TO MY BELOVED HUSBAND AND PARENTS

Abstract of thesis presented to the Senate of Universiti Putra Malaysia
in fulfillment of the requirement for the degree of Master of Science

SIGMA-DELTA ANALOG TO DIGITAL CONVERTER ON FIELD PROGRAMMABLE GATE ARRAY

By

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February 2015

Chairman: Maryam Mohd Isa, PhD
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Integrating analog to digital converter (ADC) in single system on chip (SoC) is a significant demand for portable electronic applications. Most of the input sources are in analog while the processing are in digital. ADC can be implemented in FPGA utilizing low voltage differential signaling (LVDS) available on the board. Sigma-delta ADC (SD ADC) is the best choice to be embedded in FPGA because it demands for less analog components. Integrating SD ADC in FPGA will cause to have quantization noise inside interested bandwidth which diminishes the effective number of bit (ENOB) and signal to noise and distortion (SINAD). In order to compensate the quantization noise, multi stages digital filter and high order FIR filter can be used. However, it occupies a considerable amount of logic elements (LEs) in FPGA that limits the space for main digital functions after ADC. Noise shaper sigma-delta modulator (SDM) in conjunction with hardware efficient digital filter (cascaded integrator comb, CIC) will provide not only less noise and less LE usage, but it also improves the ENOB and SINAD of the output digitized signal. The noise shaper SDM is implemented with its maximum integration. In general, the first order SD ADC consists of SD modulator (SDM), digital filter and decimation stage. Three architectures of 1^{st} order SD ADC are implemented in FPGA in this work with different SDM and digital filter topologies but with the same complexity.

The functionality of the SD ADC structure is written in verilog hardware description language (HDL). The evaluation is held in Altera Cyclone II FPGA chip on a Development and Education I (DE I) board. Comparing all the structures, it is found that noise shaper SDM with sinc filter order 2 gave the best result. The result of the 8-bit SD ADC achieves high SINAD of [45.14 dB – 39.57 dB] and ENOB of [7.21 – 6.28] bits in operative frequency bandwidth of 10 kHz. This work improves the SINAD by approximately 8.3 dB, as well as improves the ENOB by 1.37 bits increase.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia Sebagai memenuhi keperluan untuk ijazah Master Sains

ANALOG SIGMA-DELTA KEPADA PENUKAR DIGITAL PADA TATASUSUNAN PINTU MEDAN BOLEH

Oleh

MARAL FAGHANI HAMADANI

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Penyatuan penukar analog kepada digital (ADC) di dalam cip tunggal ke atas cip (SoC) adalah menjadi sesuatu yang penting dalam aplikasi elektronik mudah-alih. Kebanyakan masukan dalam aplikasi elektronik adalah dalam analog manakala pemprosesan adalah dalam bentuk digital. ADC boleh dilaksana di dalam tatasunan medan boleh program pintu (FPGA) menggunakan perbezaan isyarat voltan rendah (LVDS) yang ada pada papan. ADC sigma-delta (SD ADC) adalah pilihan terbaik untuk dibenam ke dalam FGPA kerana ia hanya memerlukan sedikit sahaja analog komponen. Persepaduan SD ADC dalam FGPA akan mengakibatkan hingar pengkuantum dalam jalur lebar yang tertentu yang seterusnya akan menghilangkan beberapa bit (ENOB) dan isyarat kepada hingar dan herotan (SINAD). Untuk mengimbangi pengkuantuman hingar, penapis digital pelbagai tertib dan penapis FIR tertib tinggi boleh digunapakai. Namun begitu, ia menggunakan beberapa elemen logik (LEs) dalam FGPA yang menghadkan ruang untuk fungsi-fungsi digital utama selepas ADC. Pembentuk hingar pemodulat sigma-delta (SDM) yang digunakan bersama dengan perisian efisien penapis digital (sesikat pengkamir melata, CIC) bukan sahaja akan mengeluarkan sedikit sahaja hingar dan kurang penggunaan LE, tetapi ia juga memperbaiki kedua-dua ENOB dan SINAD isyarat pendigitalan output. Pembentuk hingar SDM dilaksana untuk persepaduan maksimum. Secara umum, tertib pertama SD ADC mengandungi pemodulat SD (SDM), penapis digital dan peringkat perpuluhan. Tiga senibina tertib pertama SD ADC telah dilaksanakan di dalam FPGA telah dijalankan dalam kajian ini, dengan pelbagai topologi SDM dan penapis digital tetapi pada kompleksiti yang sama. Membandingkan struktur yang dicadangkan dengan dua struktur lain membuktikan bahawa struktur cadangan mempunyai kefungsian rekaan baru yang lebih baik dan dengan mengambil kira pengintegrasian yang maksimum.

Keberangkapan struktur SD ADC telah ditulis dalam bahasa perihalan perkakasan verilog (HDL). Penilaian telah dijalankan menggunakan cip Altera Cyclone II FPGA ke atas papan pembangunan dan pendidikan I (DE I). Perbandingan ke semua struktur, menunjukkan bahawa pembentuk hingar SDM dengan penapis sinc tertib 2

menunjukkan keputusan terbaik. Keputusan 8-bit SD ADC mencapai bit-bit SINAD [45.14 dB – 39.57 dB] dan ENOB [7.21 – 6.28] dalam frekuensi operasi jalur lebar berjumlah 10 kHz. Kajian ini memperbaiki SINAD sebanyak kira-kira 8.3 dB, dan juga memperbaiki ENOB melalui peningkatan sebanyak 1.37 bit.

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I certify that a Thesis Examination Committee has met on 5 February 2015 to conduct the final examination of Maral Faghani Hamadani on her thesis entitled "Sigma-Delta Analog to Digital Converter on Field Programmable Gate Array" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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LIST OF ABBREVIATIONS

A/D	Analog to Digital
AAF	Anti-aliasing filter
ADC	Analog to digital converter
ANOB	Actual number of bits
ASIC	Application-specific integrated circuit
BW	Band-width frequency
CIC	Cascaded Integrator comb filter
CLK	Clock frequency
CMOS	Complementary metal-oxide semiconductor
CT	Continues-time
DAC	Digital to analog converter
DE-I	Altera development and education FPGA board
DR	Decimation rate/Dynamic range
DSP	Digital Signal Processing
DT	Discrete-time
ENOB	Effective number of bits
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field programmable gate array
HDL	Hardware description language
I/O	Input/output
IIR	Infinite Impulse Response
LE	Logic elements
LPF	Low-pass filter
LVCMOS	Low voltage complementary metal oxide semiconductor
LVDS	Low voltage differential signaling
LVTTL	Low voltage transistor-transistor logic
MSB	Most significant bit
OSR	Oversampling ratio
PLD	programmable logic device
PWM	Pulse Width Modulation
R2R	Ladder resistor network
RC	Resistor capacitor integrator network
RTL	Register transfer level
S/H	Sample and Hold
SAR	Successive approximation register
SD	Sigma-Delta
SDM	Sigma-Delta Modulator
SFDR	Spur-free dynamic range
SINAD	Signal to noise and distortion
SNR	Signal to noise ratio
SOC	System on chip
THD	Total harmonic distortion

CHAPTER 1

INTRODUCTION

1.1 Introduction

Field-programmable gate array (FPGA) is a modern-day technology used for implementing digital designs within the digital core. Some of the advantages of FPGA over application specific integrated circuit (ASIC) chip include faster time to market, simpler design cycle and also the ability of being reprogrammed. Mostly, the signals in our surroundings are analog and need to be monitored, treated, recorded, modified or even transmitted. The origin of such signals might be from speedometer, humidity sensor, temperature sensor or other types of sensors. Most signal processing are digital-based (Carbajo & Calpe, 2014). Thus, it is required to convert the analog signal into digital for data processing.

Previously, an off-chip ADC was used to convert analog signal into digital form in FPGAs. This is space consuming and not reliable. Recently, FPGAs chip mainly equipped with various input/output (I/O) pin standard configuration such as, low voltage differential signaling (LVDS). LVDS in the FPGA can be utilized as a comparator. With the on-chip comparator, realization of ADC in FPGA is possible with minimal additional passive external components. In the recent years, implementing SD A/D converters on FPGA have received increased attention (Simple sigma-delta ADC.2010; Jimenez, Lucia, Urriza, Barragan, & Navarro, 2014a; Jimenez, Lucia, Urriza, Barragan, & Navarro, 2014b; Karmakar, Mullick, & Sinha, 2014; Mihalov & Stopjakova, 2011; Palagiri, Makkena, & Chantiagari, 2012; Syahril & Isa, 2010; Uchagaonkar, Shinde, Patil, & Kamat, 2012) compared to other types of data converter, such as flash ADC, successive approximation register (SAR) ADC and pipeline ADC. These converters for n-bit resolution utilize a considerable number of digital board requirements and off-chip components. However, the advantages of sigma-delta ADC is due to its architecture which demands for less analog components as well as less digital board equipments (Abbiati, Di Odoardo, Geraci, & Ripamonti, 2004a; J. de la Rosa, 2011; Herwies, 2014; Karmakar et al., 2014; Marker-Villumsen & Bruun, 2014; Ritoniemi, Eerola, Karema, & Tenhunen, 1990).

The advantages of first order sigma-delta ADC over multi-order SD ADC is due to its higher integration. Realization of 1st order SD ADC implementation on FPGA has been reported in few previous studies, utilizing one, integrator, single-bit comparator, sampling element, 1-bit DAC feedback loop and digital filter and decimation stage (Simple sigma-delta ADC.2010; Kaur & Singh, 2014; Palagiri et al., 2012; Sousa, Mauer, Duarte, Jasinski, & Pedroni, 2004; Uchagaonkar et al., 2012). Nevertheless, the maximum integration of noise shaper SD ADC with hardware efficient digital filter stage was not achieved in previous works. That is because the pre SD ADCs employed analog comparator outside the board as 1-bit quantizer and/or use non-noise shaper modulator with multi-stages and high order FIR filter which consumes considerable logic elements on FPGA. On the other

hand, some researches in the field, specifically focus on SDM part integration with no realization of digital filter stage (Mihalov & Stopjakova, 2011; Noor shah, 2013; Syahril & Isa, 2010) while some only focus on digital and filter decimation part for SD ADC (Kilic, Haghighitalab, Mehrez, & Aboushady, 2014; Maity & Das, 2012; Singh, Gupta, & Singh, Nov 2013). The first order sigma-delta ADC block diagram is shown in Figure 1.1. The integrator structure is responsible for quantization noise shifting to higher frequencies. It is designed differently in all the aforementioned works.

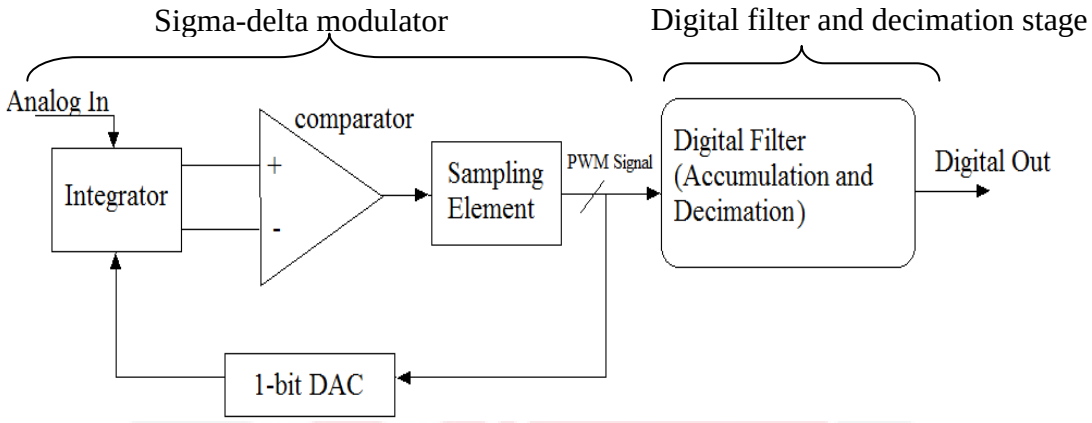

Figure 1-1. Overall block diagram of first order sigma-delta ADC

This thesis presents the integration of new SD ADC architecture on FPGA. It consists of 1st order sigma-delta modulator with noise shaping techniques, named as (SDM topology2) for its maximum integration. For digital filter stage, second order sinc filter is utilized since it is hardware efficient. To prove the performance advantages of new architecture, the results are compared with other two integrated SD ADCs with the same complexity which also done by the author of this thesis. The first architecture is 1^{st} order SD ADC with non noise shaper SDM (SDM top1) in conjunction with sinc filter order 2. The second architecture is 1^{st} order SD ADC with SDM top2 and multiplierless FIR filter. The new architecture is different from some previous published work which used non noise shaper modulator named as (SDM topology1). Previous designs with SDM topology 1 used a multi-stage complex digital filter for noise suppression to compensate for the noise remaining in interested bandwidth (Palagiri et al., 2012; Shingare & Shinde, 2014; Sousa et al., 2004; Syahril & Isa, 2010). In this structure, SDM topology 2 shaped the quantization noise to higher frequencies, hence, resulting in lowering the noise level inside the interested bandwidth. Therefore, higher signal to noise and distortion (SINAD), and effective number of bits (ENOB) are able to be achieved with less filter and decimation stage complexity. Also, sinc filter is designed and implemented to save logic element (LE) usage of FPGA board.

1.2 Problem Statement

In spite of the significant advantages of integrated SD ADCs on FPGA, noise reduction is desired to improve the dynamic performance of converter. Many factors such as switching noise, power noise and inherent noise can affect the main signal, causing to destroy the SINAD and ENOB at the ADC output. Without noise shaper SD ADC the quantization noise was distributed over the sampling frequency. In such a scenario, the signal in interested bandwidth has been seriously affected by the quantization noise. In order to overcome this problem, complex digital filter and decimation design is needed to reduce quantization noise to achieve high ENOB. However, it occupies more FPGA logic elements that cause to limit the space for the main digital functions after ADC. Also, utilizing a simple off-chip comparator instead of on-board LVDS helps to reduce the direct influence of noise on LVDS, at the output data, but it has less integration. Thus, it is finally proposed to design and implement the complete structure of SD ADC with maximum integration and hardware efficient digital filter to achieve high ENOB and SINAD at the output.

The overall performance of integrated sigma-delta type of analog to digital converters can be tackled from two different aspects, (1) sigma-delta modulator part and (2) digital filter/decimation stage. Due to the complexity of sigma-delta ADC function and digital filter and decimation requirements, it is usually either the modulator block or digital filter and decimation block mentioned in existing literature. Only a few researches have been done in the field of fulfilling the sigma-delta A/D converter with full digital techniques and further optimization toward achieving better performance (Herwies, 2014; Palagiri et al., 2012). Therefore, a new complete SD ADC implementation on FPGA is required to overcome the obstacles as mentioned in the aforementioned discussion.

1.3 Research Objective

The aim of this research is to implement a new complete SD ADC architecture on FPGA, considering maximum integration to obtain high ENOB and SINAD while using hardware efficient digital filter and decimation stage. Thus, the objectives of this thesis are as follows:

To alleviate the quantization noise involved in operative frequency with the aid of noise shaper SDM while considering its maximum integration;

To improve the resolution and applicable the output sample rate with the aid of hardware efficient digital filter and decimation stage;

To investigate the performance of proposed SD ADC architecture especially for SINAD and ENOB through constructing the noise shaper SD modulator and hardware efficient digital filter on FPGA.

1.4 Scope of Work

This research focuses mainly on ADC integration on FPGA. Thus, some basic knowledge on the basic ADC is needed. There are different types of ADCs that can be implemented on FPGA, such as SAR, pipeline and flash ADC. Among all, sigma-delta ADC has the most compatibility to be integrated in digital board due to its structure that needs the least analog components as well as digital nature functioning.

SD ADCs have different structures and various designs methods according to the order of their SDM type, complexity of digital filter, and decimation in use. They have their respective advantages and disadvantages. Despite the methods are different, but the same sigma-delta ADC type is used. Achieving high SINAD and ENOB is possessed in common with all these methods and structures. This thesis is concerned with the integration of improved architecture for first-order SD ADC on FPGA with the SDM block to shape the quantization noise outside the band of interest and single hardware efficient digital filter and decimation block to save logic elements (LEs) of FPGA. However, using complicated multi stages digital filter or complex high order FIR filter will result in the reduction of ADC noise for better signal to noise ratio (SNR). However, it is beyond the scope of this thesis.

1.5 Organization of Thesis

The thesis includes five Chapters. Chapter 1 introduces the motivation of this work, problem statement and defines the area of improvement.

Chapter 2 mainly focuses on reviewing about other published works related to this research while bringing forward the needed background information about digital ADC implementation and improvement.

Chapter 3 describes the design architecture of the proposed SDM building blocks. It explains the operation of proposed digital filter and decimation stage and prior programming before FPGA implementation.

Chapter 4 includes the both simulation results of the circuitries introduced in Chapter 3 and the experimental results for complete integrated SD A/D converter on FPGA. To prove the performance advantages of new architecture, the results are compared with other two integrated SD ADCs. The first architecture is 1^{st} order SD ADC with SDM top1 and sinc filter order 2. The second architecture is 1^{st} order SD ADC with SDM top2 and multiplierless FIR filter. Various specifications for quantifying ADC are considered such as SINAD, SNR, THD and ENOB.

Chapter 5 concludes the thesis and proposes the potential directions for future research work.

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