DETERMINISTIC AUTOMATIC TEST PATTERN GENERATION FOR BUILT-IN SELF TEST SYSTEM

By

MUHAMMAD NAZIR MOHAMMED KHALID

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Master of Science

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This thesis is dedicated to my family for their endless love,
Who encouraged and believe in me

Specially for my wife Noor Malawati Awang
Who being with me throughout my critical moment

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

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MUHAMMAD NAZIR BIN MOHAMMED KHALID

March 2006

Chairman: Roslina Mohd Sidek, PhD

Faculty: Engineering

With a great growing use of electronic products in many aspects of society, it is evident that these products must perform reliably. Their reliability depends on the testing whether or not they have been manufactured properly and behave correctly. To ease testing, digital systems are commonly designed with Built-In Self Test facility. For this reason, development of test pattern for BIST based on combination of Linear Feedback Shift Register (LFSR) and deterministic ATPG (DATPG) approach could provide more solutions, such as reduce testing time, high fault coverage and low area overhead.

One of the key challenges in BIST is the design of the Test Pattern Generation (TPG) that promised high fault coverage. The test pattern generation can be generated either manually or automatically. Problems related to ATPG are linked to the controllability and observability of the nodes in circuits. As far as the single stuck-at fault model is considered, efficient algorithms have been devised for combinational circuit. To illustrate that, the DATPG algorithm for digital combinational circuit using VHDL language is designed to generate the test patterns. Altera Max+plus II

software is used to simulate the DATPG design to achieve the minimum test patterns for digital combinational circuit. The simulation result will be presented in the form of waveform.

The results of DATPG for digital combinational circuit show that the sequence of LFSR has been reduced significantly. In BIST application, the minimum test patterns are applied to the adder/subtractor (A/S) known as circuit under test (CUT). A parallel A/S is chosen as a CUT due to the simplicity of the circuit architecture. The A/S is used to verify the proposed DATPG performance. Only one basic cell of the parallel A/S is required to determine the test pattern by considering the data flow from one cell to another. Identical test data can then be applied to both A/S inputs simultaneously. By reducing the number of test pattern, the testing time to market and manufacturing time is expected to reduce leading to reduction in the product cost.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

DETERMINISTIC AUTOMATIC TEST PATTERN GENERATION FOR BUILT-IN SELF TEST SYSTEM

Oleh

MUHAMMAD NAZIR BIN MOHAMMED KHALID

Mac 2006

Pengerusi: **Roslina Mohd Sidek, PhD**

Fakulti: **Kejuruteraan**

Oleh kerana penggunaan produk elektronik semakin meningkat dengan pesat di kalangan masyarakat, maka kebolehtahanan produk ini perlu ditingkatkan supaya ianya dapat beroperasi dengan lebih lama. Kebiasaannya kebolehtahanannya bergantung kepada pengujian untuk menentukan sama ada litar yang dihasilkan beroperasi dengan baik dan betul. Untuk memudahkan pengujian, sistem digital kebiasaannya direkabentuk dengan fasiliti "Built-In Self Test". Atas alasan ini, pembangunan corak data pengujian untuk BIST berdasarkan gabungan "Linear Feedback Shift Register (LFSR)" dan kaedah "deterministic" boleh menyediakan satu penyelesaian untuk memendekkan masa pengujian, mencapai liputan kesalahan tertinggi dan hanya menggunakan ruang litar yang minimum.

Salah satu cabaran dalam BIST ialah merekabentuk TPG yang dapat memberikan liputan kesalahan tertinggi. Corak pengujian boleh dijana secara manual ataupun secara automatik. Masalah ATPG berkaitan dengan kebolehkawalan dan pemerhatian bagi nod-nod salah suatu litar. Sekiranya model kesalahan "Stuck-at" dipertimbangkan, algorithma yang berkesan telah digunakan untuk litar kombinasi.

Oleh itu, sistem ATPG bagi litar digit menggunakan bahasa VHDL telah direkabentuk untuk menghasilkan paten pengujian. Perisian Altera MAX+plus II, digunakan dalam penyelidikan ini bagi mendapatkan paten pengujian yang minima untuk litar digit. Keputusan simulasi yang diperolehi ditunjukkan dalam bentuk gelombang.

Keputusan dari sistem ATPG untuk Litar Digit menunjukkan bahawa masa pengujian LFSR telah dipendekkan. Dalam BIST, corak pengujian yang minima digunakan keatas Penambah/Penolak yang dikenali sebagai litar yang diuji (CUT). Penambah/Penolak Selari telah dipilih sebagai CUT di sebabkan oleh rekabentuk litarnya yang ringkas. Penambah/Penolak ini digunakan untuk mengesahkan prestasi DATPG yang dicadangkan. Hanya satu sel Penambah/Penolak Selari diperlukan untuk menentukan corak pengujian dengan mengambil kira aliran data dari satu sel kepada yang lain. Data pengujian yang sama kemudian boleh dikenakan kepada kedua-dua input Penambah/Penolak secara serentak. Dengan mengurangkan paten ujian, masa untuk pemasaran dan pembuatan dijangka akan berkurang dan ini akan menjurus kepada pengurangan kos pembuatan.

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I certify that an Examination Committee has met on 1 Mac 2006 to conduct the final examination of Muhammad Nazir Mohammed Khalid on his Master of Science thesis entitled "Deterministic Automatic Test Pattern Generation for Built-In Self Test System" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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This thesis submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science. The members of the Supervisory Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

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