UNIVERSITI PUTRA MALAYSIA

RADIO FREQUENCY FRONT END RECEIVER BLOCKS WITH ULTRA LOW SUPPLY VOLTAGE AND LOW POWER DISSIPATION FOR ZIGBEE APPLICATIONS

TAN GIM HENG

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By
TAN GIM HENG

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Doctor of Philosophy

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TAN GIM HENG

April 2015

Chair: Roslina Mohd Sidek, PhD
Faculty: Engineering

Portable wireless devices have been the heat of demands in recent years for many applications such as Wireless Sensor Network (WSN) which requires low power consumption since these devices are commonly powered up by battery. One way to reduce circuit power consumption is to lower the supply voltage or DC current of the circuit. Continuous modern technology scaling with a proportional supply voltage reduction outlays a challenge in designing Radio Frequency (RF) circuits. In fact, the recent supply voltage and power consumption for mixer have been saturated at around 0.8V and 1mW respectively.

Direct conversion receiver (DCR) is the preferred choice of low power adaptation for the receiver front-end. The most common topologies for mixer are Gilbert cell, folded cascode and current bleeding mixer. However, these architectures still require high supply voltage to operate. The proposed architecture combines the current bleeding technique and folded structure to realize the operation at ultra-low supply voltage of 0.5V while enhancing the isolation between Local Oscillator (LO) and RF ports. This mixer exhibits a measured conversion gain of 11dB at the radio frequency (RF) of 2.4GHz, an input third-order intercept point (IIP3) of -0.4dBm and a LO-RF isolation measured to 60 dB and the DC power consumption is 850µW.

This research also includes the design and analysis of current bleeding mixer topology adapting forward body bias technique coupled with the integration of an inductor at the gate of the NMOS bleeding transistor to increase the conversion gain without additional DC power consumption. The measured conversion gain and IIP3 of this mixer is 13dB and -0.5dBm respectively and only consume DC power of 480µw and operates at 0.35V of supply voltage. Integrated LNA-Mixer is investigated in this thesis which focuses on ultra-low voltage and low power implementation. This integrated chip features a simulated conversion gain of 20.3dB at the radio frequency (RF) of 2.4GHz, an input third-order intercept point (IIP3) of -10.3dBm and Noise Figure (NF) is at 7.2dB. The dc power consumption is 950µw while working at the supply voltage of 0.5V.

The circuits are designed such that the critical transistors operate at optimum transconductance to meet the low power requirement of ZigBee applications. All circuits were fabricated using CMOS 0.13um technology and measurement was

performed on die samples. As a conclusion, the ultra-low voltage and low-power techniques used in this research meets the requirement for ZigBee applications while working at supply voltage of 0.5V and 0.35V with power dissipation of less than 1mW.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

BLOK PENERIMA BAHAGIAN DEPAN FREKUENSI RADIO DENGAN VOLTAN BEKALAN ULTRA RENDAH DAN PELEPASAN KUASA RENDAH UNTUK APLIKASI ZIGBEE

Oleh

TAN GIM HENG

April 2015

Pengerusi: Roslina Mohd Sidek, PhD
Fakulti: Fakulti Kejuruteraan

Permintaan peranti wayarles mudah alih meningkat kebelakangan ini untuk berbagai aplikasi seperti Rangkaian Sensor Tanpa Wayar (WSN) yang memerlukan penggunaan kuasa yang rendah kerana ianya bergantung kepada bateri. Satu cara untuk mengurangkan penggunaan kuasa litar adalah dengan mengurangkan voltan bekalan atau arus pincangan. Penskalaan teknologi modern yang berterusan berkadar dengan pengurangan voltan memberi cabaran dalam mereka bentuk litar frekuensi radio (RF). Malah, baru-baru ini, voltan bekalan dan penggunaan kuasa untuk pencampur telah masing-masing tepu pada kira-kira 0.8V dan 1mW.

Penerima Penukaran Langsung (DCR) adalah pilihan yang lebih sesuai untuk adaptasi kuasa rendah bagi penerima bahagian depan. Topologi yang biasa digunakan untuk pencampur adalah sel Gilbert, kaskod berlipat dan pencampur penyaliran arus. Walau bagaimanapun, kerangka ini masih memerlukan voltan bekalan yang tinggi untuk beroperasi. Seni bina yang dicadangkan ialah dengan menggunakan gabungan teknik penyaliran arus dan struktur berlipat untuk merealisasikan operasi pada voltan bekalan ultra-rendah di samping meningkatkan pengasingan antara pelabuhan pengayun tempatan (LO) dan RF. Pencampur ini mempamerkan gandaan penukaran yang diukur pada 11dB pada frekuensi radio (RF) 2.4GHz, satu titik input ketiga-perintah memintas (IIP3) pada -0.4dBm, pengasingan LO-RF yang diukur pada 60dB dan penggunaan kuasa DC adalah 850μW.

Tesis ini juga melaporkan reka bentuk dan analisis topologi pencampur arus penyaliran ultra kuasa rendah dan voltan rendah dengan menggunakan teknik pincangan substrat kehadapan dengan integrasi induktor di get transistor penyaliran untuk meningkat gandaan penukaran tanpa penambahan DC kuasa. Gandaan penukaran dan IIP3 pencampur adalah masing-masing 13dB dan -0.5dBm masing-masing dan hanya menggunakan kuasa DC 480μw dan beroperasi pada 0.35V voltan bekalan. LNA-pencampur bersepadu dikaji dalam tesis ini dengan memberi tumpuan kepada voltan ultra rendah dan pelaksanaan kuasa yang rendah. Pencampur bersepadu ini mempunyai gandaan penukaran 20.3dB pada frekuensi radio (RF), 2.4GHz, satu titik input ketiga-perintah memintas (IIP3) pada -10.3dBm dan angka hingar (NF) adalah di 7.2dB. Penggunaan kuasa DC adalah 950μw dengan voltan bekalan 0.5V.

Litar direka bentuk dengan memastikan transitor yang kritikal beroperasi pada transkonduktans yang optimun bagi memenuhi keperluan kuasa rendah applikasi ZigBee. Semua litar yang direka bentuk dengan menggunakan teknologi CMOS 0.13um dan pengukuran dilakukan terus pada sampel die. Kesimpulannya, voltan dan kuasa rendah teknik yang digunakan dalam reka bentuk memenuhi keperluan untuk permohonan ZigBee dan boleh beroperasi pada voltan bekalan 0.5V dan 0.35V dengan kuasa pelepasan kurang dari 1mW.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

Roslina Mohd Sidek, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Maryam Mohd Isa, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Harikrishnan Ramiah, PhD
Senior Lecturer
Faculty of Engineering
University of Malaya
(Member)

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Supervisory
Committee: **ROSLINA MOHD SIDEK**

Signature: _____
Name of
Member of
Supervisory
Committee: **MARYAM MOHD ISA**

Signature: _____
Name of
Member of
Supervisory
Committee: **HARIKRISHNAN RAMIAH**

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LIST OF ABBREVIATIONS

ADC	Analog to Digital converter
CG	Conversion gain
CMOS	Complementary Metal Oxide Semiconductor
DBM	Double-balanced mixer
DCR	Direct conversion receiver
FOM	Figure of Merit
Gm	Transconductance
IC	Integrated Circuit
IF	Intermediate frequency
IIP3	Third-Order Intercept Point
IM	Intermodulation
ISM	Industrial, Scientific, Medical
LNA	Low Noise Amplifier
LO	Local Oscillator
LPE	Layout Parasitic Extraction
LR-WPAN	Wireless personal area network
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NMOS	N-Channel MOSFET
PA	Power Amplifier
PMOS	P-Channel MOSFET
PVT	Process voltage Temperature
RF	Radio Frequency
SNR	Signal to noise ratio
SoC	System on Chip
VCO	Voltage Controlled Oscillator
V_{TH}	Threshold voltage
WLAN	Wireless local area networks
WSN	Wireless Sensor Network

CHAPTER 1

INTRODUCTION

1.1 Motivation

The desire for portability of electronic devices generated global needs for ultra-low power circuits. Ultra-low-voltage and low-power design is the main motivation for this research as increasing number of the electronics devices nowadays are wireless portable devices which are operated by the battery. Low power dissipation is very important for portable devices in order to have maximum battery life-time (Wu et al., 2007). Due to this crucial low power requirement, ultra-low voltage and low-power CMOS radio frequency integrated circuit (RFICs) has been the heat of discussion in recent years to prolong and reduce the weight of the battery (Heiberg et al., 2011).

A low-power implementation of a wireless front-end receiver had been widely reported for application such as Wireless Sensor Network (WSN) (Song et al., 2007 and Shokrani et al., 2014). WSN applications which require very low power and low data rate often adopt ZigBee standard based on the regulation of IEEE 802.15.4. This standard operates in the frequency of 2.4GHz for the short range wireless communication in WSN and very suitable for low power circuit (Manjula & Selvathi, 2012).
The basic building blocks for the RF front-end of a wireless transceiver includes low noise amplifier (LNA), mixer, filters, voltage controlled oscillator (VCO) and power amplifier (PA). One of the main challenges for low-power design for RF front-end is to achieve the desired dynamic performance while minimizing the DC power dissipation. However, minimization of the power dissipation might degrade the dynamic performance of the RF circuitry such as conversion gain and linearity. For example, reducing the DC biasing current of the mixer's transconductance stage will degrade the conversion gain and linearity of the mixer.

1.2 Problem statement

Over the years, a lot of researches have been done to meet the demand for wireless communication standard like wireless local area networks (WLAN) which require stringent specifications for high data-rate application. The IEEE 802.15.4 standard was specially developed targeted for Wireless Sensor Network (WSN) applications such as industrial automation, remote monitoring and control applications which require very low power consumption and low complexity. ZigBee standard does not impose severe restrictions on specification such as noise and sensitivity, the design restriction is more on power consumption (Cornetta, 2009). The power consumption required in WSN front-end is expected to be lower compare to other applications due to the relaxed specifications required to support a low data throughput. The focus of Wireless Sensor Network (WSN) protocols is usually on long-range and real-time applications. Low power applications that employ WSN include lighting controls, air conditioning controls, remote meter reading, security, sensors for fire safety residential and industrial automation, automotive control and monitoring, entertainment and health care. A wireless solution to the applications listed is not practical if the high power consumption in wireless devices requires frequent battery replacement or recharge. Since these applications need only low-complexity wireless connectivity with low data-rate and low-power wireless solution is feasible.

Due to the continuous CMOS technology down scaling to nano-meter level, the proportional downscaling of supply voltage is compulsory to maintain the reliability of the transistor gate-oxide (Hsieh, Lu, 2007). Scaling of CMOS technologies has a great impact on RF circuit design due to the reduction of the supply voltage (Wan, et al., 2012). The supply voltage can be reduced to around 0.5V for application with solar cells (Kousai, 2014). Figure 1.1 illustrates the trend in the supply voltage of the state-of-the-art active mixers that are published from year 1997 to 2012.

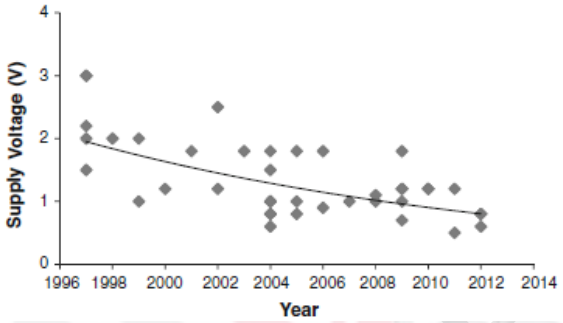

Figure 1.1: Supply voltage of reported active mixers (Shirazi et al., 2013)

As can be observed from Figure 1.1, the trend line shows that the supply voltage reduces by almost 85 mV per year and the exponential trend line tends to saturate at around 0.8V (Shirazi et al., 2013). Figure 1.2 illustrates the power consumption of the active mixer and it is obviously shows that the power consumption reduces by approximately 0.8mW per year. However, the decrease in the power consumption eventually flattens at around 1 mW which providing a bottleneck in operating the mixer in micro power range.

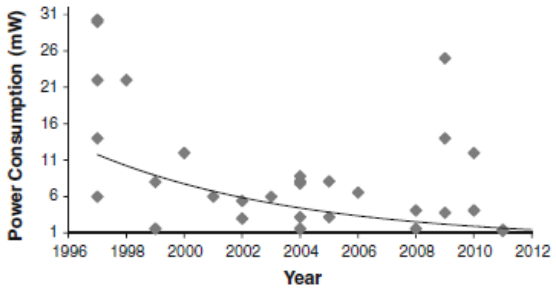

Figure 1.2: Power consumption of reported mixers (Shirazi et al., 2013)

For digital circuits, small feature size of MOSFET is preferred which is proportional to the down scaling of supply voltage. Most of the electronic system nowadays is based on System on Chip (SoC) which integrates digital, analog and RF signal on a single chip (Hong et al., 2008, and Schweiger et al., 2011). The digital circuits which are integrated with the RF circuits on the same die will require the RF circuits to operate with the same supply voltage in order to simplify the system architecture while ensuring the lowest DC power consumption (Heiberg et al., 2011). Hence, the RF

circuits must able to operate with single supply voltage in order to be compatible with the supply voltage of the digital circuit which poses a new challenge for RF circuits to operate without sacrificing the circuit's performance (Nebojsa, 2008). However, low voltage circuit design usually demands higher biasing current to avoid the dynamic range degradation which results in an increase of power consumption. Low voltage circuit design must come with low current consumption in order to reduce the overall power consumption of the circuit. Hence, low-voltage architecture coupled with low current consumption becomes very challenging to design and is an essential need for portable wireless devices. Various low-voltage and low-power design techniques have been explored and studied to enable the RF circuitry to operate at ultra-low supply voltage while maintaining the dynamic performance of the circuit. Low power consumption is one of the main specification required by ZigBee standard and can be reduced by either lowering down the supply voltage or decreasing the DC current used in the circuit.

Direct conversion receiver (DCR) is the preferred choice of low power and low cost adaptation for the receiver front-end as it directly converts the RF signal to IF signal without using the intermediate stage and external components (Chiou, Lin & Row, 2012) . This reduces the overall power consumption of the front-end receiver. One of the major issues associated with DCR is the LO to RF port isolation (Razavi, 1997). The self-mixing produces a DC offset which will degrade the performance of the receiver. Therefore, high isolation between the LO-RF ports is crucial in the effort of alleviating self-mixing (Hsu & Lee, 2006 and Yoon et al., 2011). Typically, cascoded circuit is used to enhance the isolation between the ports (Ahn et al., 2009). However, cascoded structure requires higher voltage headroom to operate and it is not suitable to be implemented for low-voltage circuits. Therefore, low-voltage mixer with high LO-RF isolation is critical for DCR architecture.

The whole system linearity of the receiver front-end is often limited by the linearity of the mixer. The input power of the mixer is relatively large compare to the input power of Low Noise Amplifier (LNA). The linearity of the mixer plays the key role to determine dynamic range of the communication system. The linearity is inversely proportional to the supply voltage and as a result to design a mixer with good linearity become very challenging nowadays as the supply voltage is scaled down to below 1V (Razavi,2007). New circuit design techniques are needed to ensure the circuit to function well while maintaining the linearity performance.

The conventional architecture of receiver front-end consists of discrete components such as low noise amplifier (LNA), mixer, voltage control oscillator (VCO), low pass filter and inter-stage matching network. The extra impedance matching circuitry leads to signal power wastage, supply power overhead and impending parasitic component due to the complexity of the circuitry. Integrated LNA-Mixer is investigated in this thesis that focus on low power implementation. As a conclusion, the ultra-low voltage and low-power techniques used in this design does not degrade the performance of the circuits and meets the requirement for ZigBee application.

1.3 Objectives

The proposed research is carried out in the effort of realizing an ultra-low voltage and low power CMOS mixer and integrated LNA-mixer in compliance with IEEE 802.15.4 ZigBee application. The proposed architectures are realized in 0.13µm, 8 metals, and 1

poly standard CMOS process. In this thesis, the primary objectives of the research are given as:

1. To investigate circuits design techniques for ultra-low voltage and low power RF front-end receiver with improved dynamic performance.
2. To design and analyze ultra-low voltage and low power new current bleeding CMOS mixer topology at 0.5V of supply voltage.
3. To enhance CMOS mixer design in term of power consumption and supply voltage headroom using inductor coupled gate bleeding transistor and forward-body bias techniques at 0.35V of supply voltage.
4. To implement and validate mixer as an integrated LNA-mixer in 0.13um technology at 0.5V of supply voltage.

1.4 Scope of Work

This thesis will focus on implementation of ultra-low voltage and low-power double balanced mixer and integrated LNA-mixer using 0.13um CMOS technology at the supply voltage of 0.5V and 0.35V. Due to the relaxed requirements of the ZigBee standard with a data rate of 250Kbps, ultra-low power consumption is the most important parameter to consider while maintaining the dynamic performance of the circuit. The dynamic performance of the mixer includes the conversion gain (CG), linearity, IIP3, Noise Figure (NF) and ports to ports isolation. These results will be compared with other reported mixers using the Figure of Merit (FOM) to prove that the proposed mixer has compatible performance while working at low supply voltage and low-power consumption.

1.5 Research methodology

Figure 1.3 illustrates the research methodology flow for the research. The circuits are designed according to the specifications and simulated using Cadence software to validate its performance. The circuits are fabricated in CMOS 0.13um technology and measurement is performed on the die using probe station to verify its performance. The proposed research is conducted with the aim of designing a ultra-low-voltage and low-power CMOS differential mixer and integrated LNA-mixer. Various low voltage and low power design technique have been studied and explored to enable the mixer to work at supply voltage of 0.5V and 0.35V.

The new CMOS current bleeding mixer is introduced by adapting a combination of NMOS-based current bleeding transistor, PMOS-based LO switching stage and integrated inductors to enable the circuit to operate with ultra-low voltage supply of 0.5V. The DC voltage required for PMOS-based LO switching stage is moving towards ground potential which is independent of positive of power supply and this makes the circuit very attractive for low voltage application. This low-voltage architecture is further utilized to enhance the isolation between the LO and RF ports while maintaining the operation with only 0.5V of supply voltage.

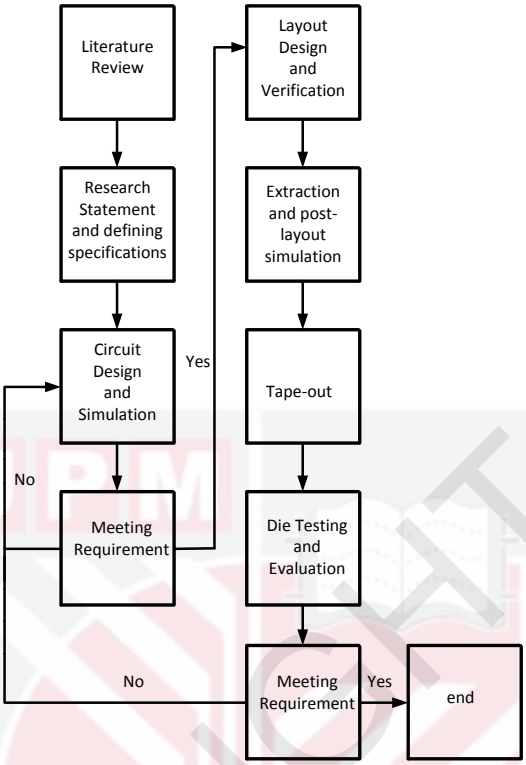

Figure 1.3: Research methodology flow

Another design approach investigated for ultra-low-power and low-voltage CMOS mixer is based on current bleeding mixer topology adapting forward body-bias technique together with the integration of inductors at the gate of bleeding transistors. This approach increases the conversion gain without increasing the DC power consumption of the circuits. Low voltage design couples with low DC current prove to be the breakthrough for micro power RF circuit design. The ultra-low voltage and low power integrated LNA-mixer that allows the sharing of DC current between LAN and mixer is also proposed which can reduce the power consumption.

1.6 Organization of the thesis

This thesis is divided into six chapters. After introducing the research objectives and challenges in chapter 1, chapter 2 starts with a review of the basic wireless receiver architectures, ZigBee standard and the fundamental operation of the mixer. This chapter also covers various topologies for low-voltage and low-power CMOS mixer and integrated LNA-mixer. All topologies are compared their performance in term of conversion gain (CG), third-order intercept point (IIP3), noise figure (NF) and port and port isolation. Chapter 3 provides an overview of the ultra-low voltage and low power mixer design at 0.5V of supply voltage in 0.13µm CMOS technology. In this chapter, a fundamental theory to implement a low-voltage mixer is discussed in depth and novel circuit design technique is introduced to improve LO-RF isolation while still able to operate at low supply voltage. The low-voltage design technique used in this circuit is further utilized to improve the IIP3 of the mixer. Ultra-low voltage mixer without

sacrificing the performance of the mixer is the key contribution from this chapter. Chapter 4 describes a further improvement in the low-voltage and low-power circuit design techniques developed in chapter 3. In this approach, forward body bias is applied to the circuit to reduce the threshold voltage of the transistor in order to reduce the overall voltage headroom of the circuit. Integrated inductor is inserted at the gate of the current bleeding transistor to increase the conversion gain of the mixer without increasing the DC biasing current of the transconductance stage. Mathematical analysis has proven that conversion gain has increased and the circuit is in stable condition as the inductor is integrated at the gate of the bleeding transistor. This mixer is able to work at ultra-low supply voltage of 0.35V. In this chapter as well, ultra-low voltage CMOS mixer with the adaptation of novel temperature compensation circuitry is discussed. The simulations results of mixer are shown and compared with the measurement results. All the experimental result of the fabricated 0.13µm CMOS mixers have been compared with the state of the arts mixer which have been published by other researchers.

Chapter 5 presents an integrated ultra-low voltage and low-power differential integrated LNA-mixer architecture. Due to the low cost requirements by the ZigBee standard, the integrated LNA-mixer will eliminate the needs of external filter and impedance matching circuitry. The DC current from mixer is reused at LNA stage to increase its transconductance for conversion gain enhancement. Furthermore, the mixer stage is folded into the LNA to reduce the voltage headroom required to operate. This integrated LNA-mixer is able to operate at the supply voltage 0.5V. In comparison respective to other reported work, the proposed architecture exhibits the lowest supply voltage headroom consumption and reports power dissipation below 1mW and this architecture proves to be among the lowest in power consumption. Finally, chapter 6 concludes the thesis with technical contributions from the work and on potential future work.

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