

UNIVERSITI PUTRA MALAYSIA

NEUTRAL-POINT-CLAMPED MULTILEVEL INVERTER DEVELOPMENT FOR TOTAL HARMONIC DISTORTION (THD) REDUCTION

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By

SHARIFAH SAKINAH BINTI TUAN OTHMAN

MASTER OF SCIENCE

UNIVERSITI PUTRA MALAYSIA

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DEDICATION

TO MY BELOVED PARENTS, MY BROTHERS, MY SISTERS, AND MY

FRIENDS.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

NEUTRAL-POINT-CLAMPED MULTILEVEL INVERTER DEVELOPMENT FOR TOTAL HARMONIC DISTORTION (THD) REDUCTION

By

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August 2014

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Over the last few decades, the Multilevel Inverter (MI) has attracted the attention of many researchers involved in this area of study. The MI is a new generation of DC-AC inverter that offers many advantages due to its features as compared to the conventional inverter as it is more suitable for handling large motor and high power applications. Mainly, it offers dv/dt stress reduction on switching devices due to its small voltage increment steps. Various methods have been used to determine the switching angle while constructing this circuit. Another favourable feature of this device is that it allows the Multilevel Inverter to operate at high voltages with low Total Harmonics Distortion (THD) without the use of a transformer.

In this work, a three phase five-level Neutral-Point-Clamped Multilevel Inverter (NPCMI) has been investigated with the focus on determining its switching angle by using a proposed new Graphical Method Analysis (GMA) in order to obtain a lower THD output voltage percentage. The triggering angle and duration of the switching devices were determined and tested in order to achieve the finest sinusoidal-like output voltage waveform. The simulation model of a three phase NPCMI was modelled and the triggering sequences were tested to validate the performance of the MI. A simulation model of the three phase NPCMI was designed and developed using the Matlab/Simulink software package to analyse the performance. The THD of the output voltages with a variable switching frequency were measured and compared with the previous three-level NPCMI and other types of MI.

In conclusion, a new technique to predict the improved switching angle of the three phase NPCMI is introduced to obtain a reduced THD output voltage waveform. The simulation has been verified by using a mathematical equation representation and also by comparison with the works of other researchers. From this work, a three phase five-level NPCMI that possesses a lower THD output voltage waveform has been successfully developed.

Abstrak thesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

PEMBANGUNAN PENYONSANG BERBILANG ARAS TITIK NEUTRAL TERAPIT UNTUK PENGURANGAN JUMLAH HEROTAN HARMONIK (JHH)

Oleh

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Pengerusi:Nashiren Farzilah Binti Mailah, PhDFakulti:Kejuruteraan

Sejak beberapa dekad kebelakangan ini, Penyonsang Berbilang Aras (PBA) telah menarik minat ramai penyelidik untuk terlibat dalam bidang ini. Penyonsang Pelbagai Peringkat (PPP) ini adalah generasi baru bagi penyonsang Arus Terus (AT)-Arus Ulang-alik (AU) yang menawarkan banyak kebaikan kerana ciri-cirinya berbanding penyonsang konvensional kerana ia lebih sesuai untuk mengendalikan motor yang besar dan aplikasi kuasa tinggi. Keutamaannya, ia menawarkan pengurangan tekanan pada dv/dt pada peranti suis kerana kenaikan kecil dalam voltan. Pelbagai kaedah telah digunakan untuk menentukan sudut pensuisan semasa membina litar ini. Satu lagi ciri yang baik daripada PBA ialah ia membolehkan PBA ini beroperasi pada voltan tinggi pada Jumlah Herotan Harmonik (JHH) yang rendah tanpa menggunakan pengubah.

Dalam kajian ini, PBA Titik Neutral Terapit Lima Aras 3-fasa telah diselidik dengan fokus untuk menentukan sudut pensuisannya menggunakan Analisis Kaedah Grafik untuk mendapatkan peratusan JHH voltan yang lebih rendah. Sudut pensuisan telah ditentukan dan diuji untuk mencapai seperti gelombang keluaran voltan yang terbaik. Model simulasi PBA Titik Neutral Terapit Lima Aras 3-fasa telah dimodelkan dan sudut pensuisan telah diuji untuk mengesahkan prestasi PBA.

Model simulasi PBA Titik Neutral Terapit Lima Aras 3-fasa telah direka dan dibangunkan menggunakan pakej perisian Matlab/Simulink untuk menganalisis prestasinya. JHH keluaran voltan dengan berbilang sudut pensuisan diukur dan dibandingkan dengan tiga tahap bertingkat Penyonsang Berbilang Aras (PBA) Titik Neutral Terapit Lima Aras 3-fasa sebelumnya dan lain-lain jenis PBA

Sebagai kesimpulan, satu teknik baru untuk meramalkan sudut pensuisan yang ditambah baik diperkenalkan kepada PBA Titik Neutral Terapit Lima Aras 3-fasa untuk mendapatkan JHH keluaran gelombang voltan yang dikurangkan. Simulasi telah disahkan dengan perisian simulasi Matlab/Simulink dan juga dibandingkan dengan hasil

kerja lain-lain penyelidik. Dari kerja-kerja ini, PBA Titik Neutral Terapit Lima Aras 3fasa bertingkat yang mempunyai gelombang keluaran voltan yang rendah Jumlah JHH telah berjaya dibangunkan.



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I certify that a Thesis Examination Committee has met on 18th February 2014 to conduct the final examination of Master Science on her thesis entitled "**Neutral-Point-Clamped Multilevel Inverter Development for Total Harmonic Distortion (THD) Reduction**" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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LIST OF ABBREVIATIONS

AC	Alternating Current
APODPWM	Alternative Phase Opposition Disposition Pulse Width Modulation
CCMLI	Cascaded Cell Multilevel Inverter
DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
DTC	Direct Torque Control
EMI	Electromagnetic Interference
ESWM	Equal Step Width Method
EV	Electric Vehicle
FCMI	Flying Capacitor Multilevel Inverter
FFT	Fast Fourier Transform
HV	High Voltage
HVDC	High Voltage Direct Current
GMA	Graphical Method Analysis
IEEE	Institute of Electrical and Electronics Engineering
IGBT	Insulated Gate Bipolar Thyristor
ICDI	Line Current
MI	Multilevel Inverter
MSWM	Modified Step Width Modulation
MV	Medium Voltage
NPCMI	Neutral-Point-Clamped Multilevel Inverter
PBA	Penyonsang Berbilang Aras
PDPWM	Phase Disposition Pulse Width Modulation
PODPWM	Phase Opposition Disposition Pulse Width Modulation
PWM	Pulse Width Modulation
R	Resistive
RL	Resistive Inductive
SHE	Selective Harmonics Elimination
SVM	Space Vector Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
TCHB	Transistor Clamped H-Bridge
THD	Total Harmonics Distortion
VDC	Voltage Direct Current
UPFC	Unified Power Flow Controller
V _{LN}	Line-to-neutral Voltage
V LN V _{LL}	Line-to-line Voltage
VSI	Voltage Source Inverter
101	voltage Source inverter

LIST OF SYMBOL

- $_{\circ}^{\Omega}$
- ohm degree omega micro angle ω
- μ
- α



CHAPTER 1

INTRODUCTION

1.1 Background

Today, the utilisation of multilevel inverters (MI) has become wider when compared to the existing two-level voltage source inverters (VSI) in the power industry especially in high voltage and high power applications. This type of multilevel inverter offers high efficiency and reduced production costs which are greatly desired in the industry. Generally, the multilevel inverter operates by synthesising a desired output voltage from several levels of DC voltages or DC supplies. At low voltage, the conventional twolevel VSI are sufficient. However, the situation changes when it comes to medium voltage (MV) and high voltage (HV). By using a multilevel inverter, more than two levels of the output voltage can be achieved with a smoother and less distorted waveform with a low Total Harmonics Distortion (THD) value [1]. A desired output voltage waveform can be collectively obtained from a MI with the desirable features of less distortion, low switching frequency, higher efficiency, and lower voltage devices.

The uniqueness of the MI structure allows it to be operated at higher voltages without the use of a power transformer. As the number of the MI level increases, the harmonic content of the output voltage waveform decreases significantly [2 and 3]. There are three main topologies for MI; neutral-point-clamped, flying capacitor [4] and H-bridge cascaded [5, 6, 7 and 8]. These topologies are classified by the structures that are used in each construction. Each topology offers its own advantages and disadvantages which make it different in aspects of application.

Among these three topologies, the Neutral-Point-Clamped Multilevel Inverter (NPCMI) is the most widely used in all areas of industry. This topology was first proposed by A. Nabae, I. Takashi and H. Akagi [9]. Basically, NPCMI operates by producing a small step of staircase output voltage from several levels of DC capacitor voltages and can be extended to a higher level so that it is able to reach a higher AC voltage output. Therefore NPCMI can be constructed to produce a greater amount of smaller voltage steps that in the end will be similar to a sinusoidal waveform.

As harmonics are one of the issues in power quality that usually occurs in a power system network, the need to reduce harmonics is significant. In a standard Alternating Current (AC) power system, the harmonics occur at a multiple of the fundamental frequency which is either at a fundamental frequency of 50 Hz or 60 Hz. Harmonic distortion can be found both in voltage and current waveforms which is caused by electronic component loads or in common wiring systems according to Ohm's Law. THD can be defined as a ratio of the sum (as a percentage) of all harmonic components to the fundamental frequency component. As applied to a power system, a lower THD means a reduction of harmonics to the lowest percentage.

1.2 Problem Statement

In previous years, MI has been used as a replacement for conventional VSI, whether it is in a power system or in machinery applications. In a low voltage application, there is nothing of concern if the conventional VSI is employed. However, this is not the case when VSI is used in medium or high power applications. Even though many research studies have been conducted in this area, there is still some rooms for improvement. One of the improvements of interest to researchers is to obtain an output voltage with lower THD values. A result from previous work (Chaturvedi, Jain and Agrawal, 2005, Zambra et al., 2008, Panagis et al., 2008 and Mailah et al., 2009) showed that the values of the output voltage THD are higher compared to the value stated by the IEEE STD 519-1992 by using different method of finding switching angle [10, 11, 12 and 13]. According to the *IEEE* standard, the number of levels of a multilevel inverter should be increased in order to obtain an output waveform similar to a sinusoidal waveform so that the THD is reduced. The standard mentioned 5 % as the limit for the THD value [14]. Previously, the existing method to calculate the switching angle like space vector modulation (SVM), pulse width modulation (PWM) and others are complicated method to determine approximate switching angle that give low THD.

The motivation for this current work is to obtain an output voltage waveform with a low THD value. This is to be achieved through the determination of the switching angle of the power electronic devices by proposing a new technique of predicting the switching angle. The research topic is important as it provides an alternative and simpler method of calculating the switching angle that can produce an output voltage waveform with a smaller THD compared to the existing methods which are more complicated in order to determine the switching angle.

Another motivation is that based on previous work by Sayago *et al.*, one of the less attractive features of NPCMI is its relatively high switching losses which limit the switching frequency up to 1050 Hertz [15]. So in this work, the designed NPCMI is simulated under various switching frequencies ranging from 50 Hz to 1000 Hz to analyse the stability of this NPCMI when subjected to changes in switching frequency.

1.3 Aim and Objectives

The aim of this work is to propose a new method to determine suitable switching angle called Graphical Method Analysis (GMA) in order to achieve a lower THD output voltage value.

There are three main objectives of this research. These objectives are listed as follows:

- 1. To model a simulation circuit of a three-phase five-level NPCMI using the Matlab/Simulink simulation software.
- 2. To propose and test the performance of GMA used in determining the switching angle of three phase five-level NPCMI and analyze the harmonics contents of the output voltage.

3. To investigate the stability of a three-phase five-level NPCMI when subjected to varying switching frequencies.

1.4 Scope of Work

Based on the previous work of a three-phase three-level NPCMI [13], this work is expanded to design and model a three-phase five-level NPCMI using the Matlab/Simulink simulation software. The main aim of this work focuses on a simulation model to determine the switching angle using the new proposed method. It begins with the design of a three-phase five-level NPCMI and then calculates and determines the switching angle of each power electronic switch parameter. Graphical Method Analysis (GMA) is proposed and applied in this work. The calculated switching angles are applied and the associated THD of the output voltage waveforms are noted. The total harmonic distortion (THD) is observed at each step while running the simulation. The THD value obtained from this work is compared to other works related to this design. Subsequently a higher level is constructed to prove the proposed method is useable to achieve the best output waveform. The switching frequency is varied from 50 Hz to 1000 Hz and the THD is observed to determine the stability of the proposed system.

1.5 Contributions

The contributions of this work are:

- 1. Graphical Method Analysis (GMA) has been proposed in this work for a three-phase NPCMI and has been simulated and validated using Matlab/Simulink simulation software. This method can be used to obtain the best output waveform to achieve a lower THD value compared to other existing methods.
- 2. The stability of the NPCMI has been analysed and shown to be stable for a switching frequency ranging from 50 Hz to 1000 Hz.

1.6 Thesis Layout

This thesis is organised in five chapters. Chapter 1 introduces the background of the project, gives the problem statement, scope of works and the aims and objectives of the research. The contributions of this work are also stated.

Chapter 2 presents a literature review related to the study. It begins with a discussion on MI focusing on NPCMI and also a few reviews of other topologies, control strategies, THD, applications of MI and a conclusion of the literature review. Several research works concerning published results are also considered as a reference in developing the proposed graphical method for a three-phase NPCMI.

Chapter 3 explains the research methodology that is used to obtain the results from this project. First of all, the basic principles and structure of this three-phase five-level

NPCMI are explained. Then the modelling of the three-phase five-level NPCMI is constructed by using the Matlab/Simulink software. Furthermore, the GMA of this structure is created to provide a comparison with the results of other research works. Then, the method is expanded to a three phase seven-level NPCMI. Finally, the design of the NPCMI is simulated under varying switching frequencies in order to investigate the performance and stability.

Chapter 4 presents the results of this work. Firstly, the results of the construction and calculation of the graphical method analysis (GMA) of the three-phase five-level NPCMI are shown, analysed and discussed. The total harmonic distortion of the output voltage waveform of this structure is observed and compared to previous work to ensure that this research has improved the situation. Then the three-phase seven-level NPCMI results using the same graphical method analysis technique are analysed to prove that a higher level of NPCMI will produce a better output and the proposed method is valid. The switching frequency is varied to observe the stability of the system. All results obtained are discussed and described.

Finally, Chapter 5 concludes the overall research of the construction and analysis result of this three-phase five-level NPCMI. This chapter also includes a few recommendations that can be implemented in this research area in the future.



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APPENDICES

A: Parameters for each devices:

1. Filter, L

Block Param		
-Parallel RLC Bran		
	allel branch of RLC elements. ype' parameter to add or remove elements from the bran	ch.
Parameters		
Branch type: 📘		~
Inductance L (H)	:	
100e-3		
📃 Set the initial	inductor current	
Measurements	None	~
	OK Cancel Help	Apply
capacitor		

2. DC capacitor

🐱 Block Para	meters: C1	
-Parallel RLC Bra	anch (mask) (link)	
	arallel branch of RLC elements. h type' parameter to add or remove elements from the branch	٦.
Parameters		
Branch type:	c	~
Capacitance C	(F):	
2200e-6		
📃 Set the initi	ial capacitor voltage	
Measurements	None	~
	OK Cancel Help A	Apply

3. Diode Clamped

Diode (mask) (link) Implements a diode in parallel with a series RC snubber circuit. In on-state the Diode model has an internal resistance (Ron) and inductance (Lon). For most applications the internal inductance should be set to zero. The Diode impedance is infinite in off-state mode. Parameters Resistance Ron (Ohms) : 0.001 Inductance Lon (H) : 0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Cs (F) : 0 Snubber capacitance Cs (F) : 0 Show measurement port	🐱 Bl	ock Parameters: DC1 🛛 🔀
In on-state the Diode model has an internal resistance (Ron) and inductance (Lon). For most applications the internal inductance should be set to zero. The Diode impedance is infinite in off-state mode. Parameters Resistance Ron (Ohms) : 0.001 Inductance Lon (H) : 0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0 Show measurement port	Diod	e (mask) (link)
Resistance Ron (Ohms) : 0.001 Inductance Lon (H) : 0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0	In or For n	n-state the Diode model has an internal resistance (Ron) and inductance (Lon). Most applications the internal inductance should be set to zero.
0.001 Inductance Lon (H) : 0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0 Show measurement port	Para	meters
Inductance Lon (H) : 0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0 Snubber capacitance Cs (F) :	Resi	stance Ron (Ohms) :
0 Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0	0.0	01
Forward voltage Vf (V) : 0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0	Indu	ictance Lon (H) :
0.7 Initial current Ic (A) : 0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0	0	
Initial current Ic (A) : Initial current Ic (A) : Snubber resistance Rs (Ohms) : Inf Snubber capacitance Cs (F) : Inf Snubber capacitance Cs (F) : Inf	Forv	vard voltage Vf (V) :
0 Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0	0.7	
Snubber resistance Rs (Ohms) : inf Snubber capacitance Cs (F) : 0 Show measurement port	Initia	al current Ic (A) :
inf Snubber capacitance Cs (F) : 0 Show measurement port	0	
Snubber capacitance Cs (F) : 0 Show measurement port	Snut	ober resistance Rs (Ohms) :
0 Show measurement port	inf	
Show measurement port	Snut	ober capacitance Cs (F) :
	0	
OK Cancel Help Apply	2	5how measurement port
		OK Cancel Help Apply

4. Anti-parallel Diode

🖬 Block Parameters: D1a 🛛 🔀
Diode (mask) (link)
Implements a diode in parallel with a series RC snubber circuit. In on-state the Diode model has an internal resistance (Ron) and inductance (Lon). For most applications the internal inductance should be set to zero. The Diode impedance is infinite in off-state mode.
Parameters
Resistance Ron (Ohms) :
0.001
Inductance Lon (H) :
0
Forward voltage Vf (V) :
0.8
Initial current Ic (A) :
0
Snubber resistance Rs (Ohms) :
inf
Snubber capacitance Cs (F) :
Show measurement port
OK Cancel Help Apply

5. IGBT

C

🐱 Block Parameters: s1a	\times
_IGBT (mask) (link)	
Implements an IGBT device in parallel with a series RC snubber circuit. In on-state the IGBT model has internal resistance (Ron) and inductance (Lon). For most applications, Lon should be set to zero. In off-state the IGBT model has infinite impedance.	
Parameters	
Resistance Ron (Ohms) :	
0.001	
Inductance Lon (H) :	
0	
Forward voltage Vf (V) :	
1	
Current 10% fall time Tf (s) :	=
1e-6	
Current tail time Tt (s):	
2e-6	
Initial current Ic (A) :	
0	
Snubber resistance Rs (Ohms) :	
1e5	
Snubber capacitance Cs (F) :	
inf	
Show measurement port	
OK Cancel Help Apply	

6. Pulse Generator

Source Block Pa	rameters: PG1a	
-Pulse Generator		
Output pulses:		
$\begin{array}{l} \mbox{if } (t >= \mbox{PhaseDelay}) \\ \mbox{Y}(t) = \mbox{Amplitude} \\ \mbox{else} \\ \mbox{Y}(t) = \mbox{0} \\ \mbox{end} \end{array}$	X& Pulse is on	
Pulse type determines	the computational technique used.	
Time-based is recomm is recommended for us model using a variable	ended for use with a variable step s e with a fixed step solver or within step solver.	solver, while Sample-base a discrete portion of a
Parameters		
Pulse type: Time bas	ed	~
Time (t): Use simulat	ion time	~
Amplitude:		
2		
Period (secs):		
0.02		
Pulse Width (% of pe	iod):	
PWS1a		
Phase delay (secs):		
TS1a		
☑ Interpret vector p	arameters as 1-D	
	ОК	Cancel Help

B: *m*-file coding

1. Three phase five-level NPCMI

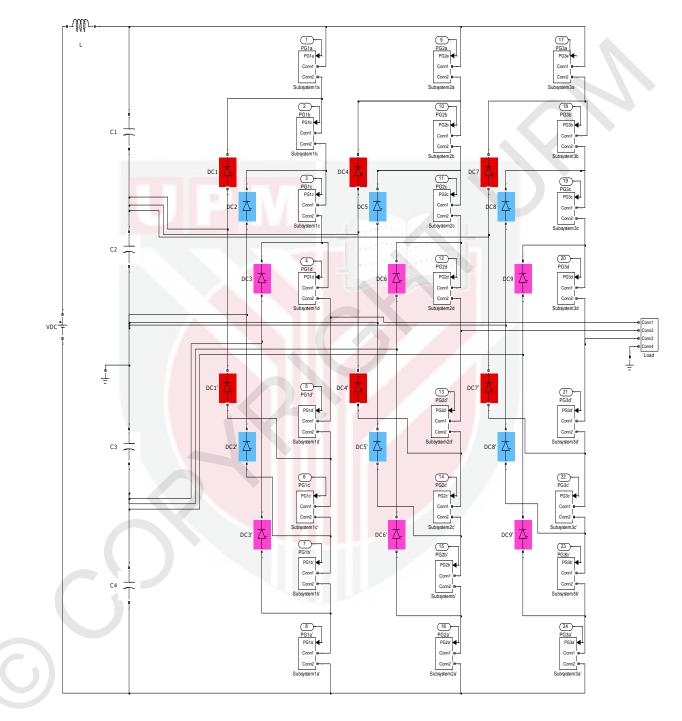
```
%a-d: Pulse width
%e-f: Phase Delay
a=110;
b=165;
c=360-b;
d=360-a;
e=(90-(a/2));
f=(90-(b/2));
q=(90+(a/2));
h=(90+(b/2));
i=(180+f);
j=(180+e);
%Pulse Width (Switching Duration) in percent (%)
PWS1a = (a)*(100/360); PWS1b = (b)*(100/360); PWS1c = (c)*(100/360); PWS1d = (d)*(100/360);
PWS2a = (a)*(100/360); PWS2b = (b)*(100/360); PWS2c = (c)*(100/360); PWS2d = (d)*(100/360);
PWS3a = (a)*(100/360); PWS3b = (b)*(100/360); PWS3c = (c)*(100/360); PWS3d = (d)*(100/360);
PWS1_a = (a)*(100/360); PWS1_b = (b)*(100/360); PWS1_c = (c)*(100/360); PWS1_d = (d)*(100/360);
PWS2_a = (a)*(100/360); PWS2_b = (b)*(100/360); PWS2_c = (c)*(100/360); PWS2_d = (d)*(100/360);
PWS3[a = (a)*(100/360); PWS3[b = (b)*(100/360); PWS3[c = (c)*(100/360); PWS3[d = (d)*(100/360); PWS3
%Phase Delay in sec
TS1a = (e)*(0.02/360);
                                                                TS2a = ((e)+(120))*(0.02/360);
                                                                                                                                                     TS3a = ((e) + (240)) * (0.02/360);
TS1b = (f) * (0.02/360);
                                                                TS2b = ((f) + (120)) * (0.02/360);
                                                                                                                                                     TS3b = ((f) + (240)) * (0.02/360);
TS1c = (-f) * (0.02/360); TS2c = ((-f) + (120)) * (0.02/360);
                                                                                                                                                     TS3c = ((-f) + (240)) * (0.02/360);
TS1d = (-e)*(0.02/360); TS2d = ((-e)+(120))*(0.02/360);
                                                                                                                                                     TS3d = ((-e) + (240)) * (0.02/360);
TS1_d = (g) * (0.02/360); TS2_d = ((g) + (120)) * (0.02/360);
                                                                                                                                                     TS3_d = ((g) + (240)) * (0.02/360);
TS1_c = (h) * (0.02/360); TS2_c = ((h) + (120)) * (0.02/360);
                                                                                                                                                     TS3_c = ((h) + (240)) * (0.02/360);
TS3_b = ((i) + (240)) * (0.02/360);
TS1 a = (j) * (0.02/360);
                                                                TS2 a = ((j)+(120))*(0.02/360);
                                                                                                                                                     TS3_a = ((j) + (240)) * (0.02/360);
```

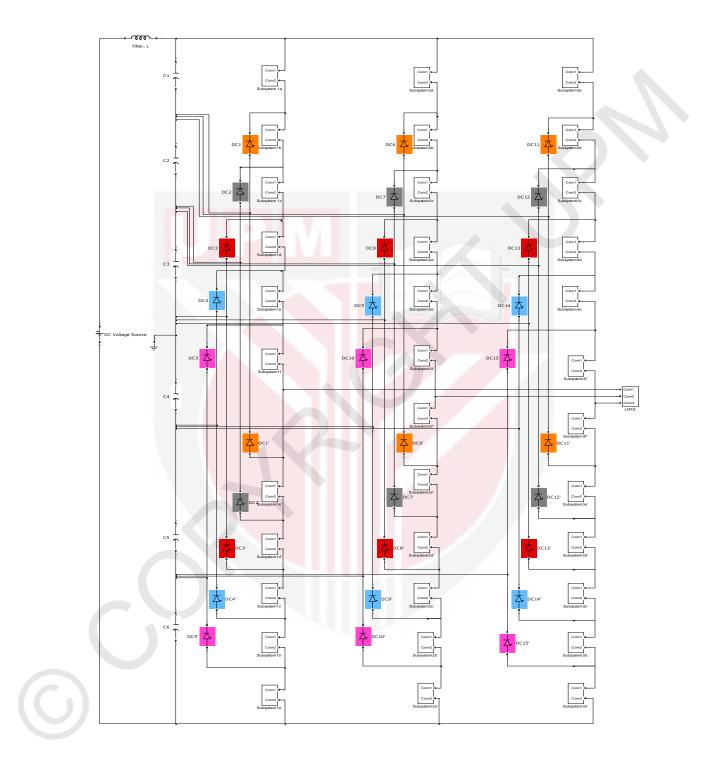
2. Three phase seven-level NPCMI

%a−f: Pulse Width						
%g-o: Phase Delay						
a=61;						
b=110;						
c=150;						
d=190;						
e=230;						
f=270;						
g=(90-(a/2));						
h=(90-(b/2));						
i=(90-(c/2));						
j=(90+(a/2));						
k = (90 + (b/2));						
1=(90+(c/2));						
m=(180+i);						
n=(180+h);						
o=(180+g);						
Pulse Width (Switching Du	uration) in percent(%)					
PWS1a = (a)*(100/360); H	PWS1b = (b)*(100/360);	PWS1c = (c) * (1)	.00/360); PWS1d	= (d) *(100/360);	PWS1e = (e)*(100/360);	PWS1f = (f)*(100/36
	PWS2b = (b)*(100/360);	PWS2c = (c)*(1		= (d) *(100/360);	PWS2e = (e)*(100/360);	PWS2f = (f)*(100/36
PWS3a = (a)*(100/360); H	PWS3b = (b)*(100/360);	PWS3c = (c) * (1)		= (d) *(100/360);	PWS3e = (e)*(100/360);	PWS3f = (f)*(100/36
$PWS1_a = (a) * (100/360); H$	PWS1_b = (b)*(100/360);	$PWS1_c = (c) * (1)$.00/360); PWS1_d	= (d) *(100/360);	PWS1_e = (e)*(100/360);	$PWS1_f = (f) * (100/36)$
$PWS2_a = (a) * (100/360); H$	PWS2_b = (b)*(100/360);	PWS2c = (c) * (1)	.00/360); PWS2_d	= (d) *(100/360);	PWS2_e = (e)*(100/360);	PWS2_f = (f)*(100/36
PWS3_a = (a)*(100/360); H	PWS3_b = (b) *(100/360);	$PWS3_c = (c) * (1)$.00/360); PWS3_d	= (d)*(100/360);	PWS3_e = (e)*(100/360);	PWS3_f = (f)*(100/36
*Phase Delay in sec						
TS1a = $(q) * (0.02/360);$	$T_{220} = ((\alpha) + (120)) * (0)$	02/2601 78	a - ((a) (240));	t/0 02/2601.		
	TS2a = ((g) + (120)) * (0)		3a = ((g)+(240))			
TS1b = (h) * (0.02/360);	TS2b = ((h) + (120)) * (0)	-	$3b = ((h) + (240))^{3}$			
TS1c = (i)*(0.02/360);	TS2c = ((i) + (120)) * (c)		$BC = ((i) + (240))^{3}$			
TS1d = (-i)*(0.02/360);	TS2d = ((-i)+(120))*(0.02/360); TS:	3d = ((-i) + (240))	*(0.02/360);		
TS1e = (-h)*(0.02/360);	TS2e = ((-h)+(120))*(0.02/360); TS	Be = ((-h) + (240))	*(0.02/360);		
TS1f = (-g)*(0.02/360);	TS2f = ((-g)+(120))*(0.02/360); TS:	Bf = ((-g) + (240))	*(0.02/360);		
TS1 f = (j)*(0.02/360);	TS2 f = ((j)+(120))*(C	.02/360); TS:	$f = ((j) + (240))^{3}$	۲(0.02/360);		
TS1 e = (k)*(0.02/360);	TS2 = ((k) + (120)) * (0)	.02/360); TS:	$B = ((k) + (240))^{3}$	t(0.02/360);		
TS1 d = (1)*(0.02/360);	TS2 d = ((1)+(120))*(0		$d = ((1) + (240))^{3}$			
TS1 c = (m) * (0.02/360);	TS2 c = ((m) + (120)) * (0)		$3 c = ((m) + (240))^{3}$			
	_		-			
$TS1_b = (n) * (0.02/360);$	$TS2_b = ((n)+(120))*(0)$ $TS2_a = ((0)+(120))*(0)$.02/300); 15	3_b = ((n)+(240)); 3 a = ((o)+(240));	(0.02/300);		

C: Matlab/Simulink Circuit

1. Three phase five-level NPCMI





2. Three phase seven-level NPCMI

BIODATA OF STUDENT

Sharifah Sakinah Tuan Othman was born on 8th of July 1983. Her primary education started at Sekolah Rendah Islam, Sungai Ramal Dalam, Kajang, Selangor. Later, she managed to pursue her studies in secondary school at Sekolah Menengah Kebangsaan Jalan Tiga, Bandar Baru Bangi, Selangor. Then, she continued secondary school at Sekolah Menengah Teknik Port Dickson. She started her higher educacation at Ungku Omar Polytechnic, Ipoh in Diploma of Electronic. She has received her B. Eng. of Electrical and Electronics Engineering from Universiti Putra Malaysia in 2008. She has an experience working as a research assistant in Universiti Putra Malaysia for a year involving in power electronics and as a demonstrator for Electrical and Electronic Technology Laboratory start from July 2009 to June 2013. In June 2009, she further studies for Master Degree in Electrical Power Engineering at Universiti Putra Malaysia.



LIST OF PUBLICATIONS

Journal

1. Sh. Sakinah. T. Othman, Nashiren F. Mailah and I. Aris, New Technique of Predicting of Switching Angle For Three Phase Neutral-Point-Clamped Multilevel Inverter, *Journal of Engineering Science and Technology*, School of Engineering, Taylor's University, 2013.

Proceedings

- 1. Nashiren. F. Mailah, M. Suhairy Saidin and Sh. Sakinah. T. Othman, Simulation and Construction of Single Phase Flying Capacitor, *IEEE Student Conference on Research and Development (SCOReD) 2011*, IOI Palm Garden Resort, Putrajaya, Malaysia, 13th-14th December 2010.
- 2. Nashiren F. Mailah, Sh. Sakinah T. Othman, H. Tsuyoshi and Y. Hiroiki, Harmonics Reduction of Three Phase Five-level Neutral-Point-Clamped Multilevel Inverter, *IEEE Conference on Power and Energy (PECon)*, 2nd -5th December Kota Kinabalu, Sabah, Malaysia, 2012.
- Nashiren F. Mailah, Sh. Sakinah T. Othman, I. Aris, M. Norhisam, T. Hanamoto, H. Yamada, Determination of Triggering Angle through Graphical Method Analysis, UPM-KIT Symposium of Applied Engineering Science (SAE 2013), Universiti Putra Malaysia, 30th Sept-1st Oct 2013.