UNIVERSITI PUTRA MALAYSIA

DESIGN OF 1K ASYNCHRONOUS STATIC RANDOM ACCESS MEMORY USING 0.35 MICRON COMPLEMENTARY METAL OXIDE SEMICONDUCTOR TECHNOLOGY

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YEONG TAK NGING

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Chairman : Roslina Mohd Sidek, PhD

Faculty : Engineering

Static Random Access Memory (SRAM) is a high speed semiconductor memory which is widely used as cache memory in microprocessors and microcontrollers, telecommunication and networking devices.

The SRAM operations are categorized into two main groups: asynchronous and synchronous. A synchronous SRAM has external clock input signal to control all the memory operation synchronously at either positive or negative edge of the clock signal. While, in asynchronous SRAM, the memory events are not referred or controlled by the external clock.

In this study, we have proposed an asynchronous SRAM which configured with a self-holding system in the control unit. The self-holding SRAM control system can produce appropriate signals internally to operate the SRAM system automatically, eliminating hold and wait time, and eliminating Sense Enable and Output Enable signals which usually used in SRAM control system. All input

signals are synchronized by the internal control unit. The overall SRAM operations however do not depend on the rising of falling edge of the global (external) clock signal, and thus, the design is still categorized under asynchronous SRAM.

The proposed self-holding control system has been developed for a 1 kilobit SRAM using MIMOS 0.35 micron 3.3V CMOS technology Due to limited computer resources such as speed and space, the design had been limited to 1 kilobit memory size. The design covers both schematic and layout designs using Hspice and Cadence Layout Editor, respectively. Meanwhile analysis covers Hspice, Timemill and LVS (Layout versus Schematic).

The simulation results have shown the self-holding SRAM control system was working successfully. The design operation speed was 7.0% faster as compared to the SRAM system without the self-holding circuit. An operation speed of 66Mhz with access time of 2.85ns was achieved.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

REKABENTUK LITAR TAK SEGERAK 1K *STATIC RANDOM ACCESS MEMORY* DENGAN MENGGUNAKAN TEKNOLOGI *COMPLEMENTARY METAL OXIDE SEMICONDUCTOR* 0.35 MIKRON

Oleh

YEONG TAK NGING

April 2005

Pengerusi : Roslina Mohd Sidek, PhD

Fakulti : Kejuruteraan

SRAM atau "*Static Random Access Memory*" merupakan ingatan semikonduktor yang berkelajuan tinggi di man ia digunakan secara meluas sebagai ingatan utama dalam litar pemprosesan mikro, litar pengawalan mikro, telekomunikasi dan peranti rangkaian.

Operasi *SRAM* dapat dikategorikan dalam dua kumpulan utama, iaitu litar tak segerak and litar segerak. *SRAM* segerak mempunyai kawalan masukan berjam luaran bagi mengawal kesemua operasi secara segerak samada pada pinggir positif atau pinggir negatif. Sementara itu, dalam *SRAM* tak segerak, operasinya tidak merujuk atau dikawal oleh kawalan berjam luaran.

Dalam kajian ini, kami mencandangkan satu litar *SRAM* tak segerak dengan litar pegang-sendiri. Sistem kawalan bagi sistem *SRAM* tersebut dapat menjana keluaran yang sepatutnya secara dalaman bagi mengoperasi *SRAM* secara automatik, menghapuskan masa pegang dan masa menunggu, serta menghapuskan

masukan "Deria Dibenarkan" dan "Keluaran Dibenarakan". Semua masukan disegerakkan oleh unit kawalan dalaman. Namun, keseluruhan operasi *SRAM* tidak bergantung kepada pinggir positif atau pinggir negatif masukan berjam, dan dengan demikian, ia masih dikenali sebagai *SRAM* tak segerak.

Sistem kawalan yang dicandangkan dibina untuk 1 kilobit sistem *SRAM* dengan menggunakan teknologi MIMOS 0.35 mikron 3.3V *CMOS*. Disebabkan oleh keterhadan kelajuan komputer dan simpanannya, rekabentuk telah diterhadkan kepada ingatan bersaiz 1 kilobit sahaja. Rekabentuk merangkumi litar dan bentangan dengan menggunakan *Hspice* dan *Cadence Layout Editor* masing-masing. Sementara itu, analisi merangkumi *Hspice*, *Timemill* dan *LVS* (Bentangan lawan Litar).

Simulasi telah menunjukkan sistem kawalan pegang-sendirir *SRAM* tersebut berjaya berfungsi. Rekabentuk tersebut berfungsi dengan 7.0% lebih laju berbanding dengan sistem tanpa kawalan pegang-sendiri. Kelajuan operasi adalah 66Mhz dengan masa capaian bernilai 2.85ns.

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LIST OF ABBREVIATIONS

μBGA	Micro Ball Grid Array
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
NMOS	n-channel depletion Metal Oxide Semiconducto
CSP	Chip Scale Package
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
DRC	Design Rules Checker
EEPROM	Electrical Erasable Read Only Memory
ERC	Electrical Rules Checker
ESD	Electro Static Discharge
FBGA	Fine-pitch Ball Grid Array
FeRAM	Ferroelectric Random Access Memory
I/O	Input/Output
IC	Integrated Circuit
LVS	Layout Versus Schematic
LW	Late Write
MRAM	Magnetoresistive Random Access Memory
NMOS	n-type Metal Oxide Silicon
PB	Pipelined Burst
ROM	Read Only Memory
SRAM	Static Random Access Memory
sTSOP	Shrink Thin Samll Outline Package
TFT	Thin Film Transistor
TSOP	Thin Small Outline Package
μBGA	Micro Ball Grid Array
W/L	Width/Length
ZBT	Zero Bus Turn-around

CHAPTER 1

INTRODUCTION

1.1 Semiconductor Memories

Semiconductor memories have a wide market and commercial values. Semiconductor memories are divided into two families; volatile and non-volatile. Volatile memories are able to retain the data in the device as long as the power is supplied. For non-volatile memories, the data can retain in the device after the cutoff of the power supply. As an example, Read Only Memory (ROM) is a non-volatile memory while Random Access Memory (RAM) is a volatile memory. Recently, combination of volatile and non-volatile memories has been highly applied especially in critical operation such as networking and workstation. Various types of semiconductor memories have been introduced in almost all kind of electrical products ranging from home products to networking and communication products. Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Electrical Erasable Read Only Memory (EEPROM), Double Data Rate DRAM (DDRRAM), Dual Channel DDRRAM, Rambus, Magnetic Random Access Memory (MRAM), Flash memory, Ferro-Electric Random Access Memory, Mirror Bit Random Access Memory, and so on.

Due to the high demand of semiconductor memories for consumers, semiconductor technologies continue to scale down to achieve higher density and higher performance.

1.2 SRAM

Static Random Access Memory (SRAM) is a very fast and low power memory. It consists of latch type cells where refresh circuitry is not required. Refresh circuitry is needed in DRAMs (Dynamic Random Access Memory) to retain the stored data. The refresh system in DRAM requires complex design and engineering sophistication [1]. For SRAM, data are stored in the memory cells as long as voltage is supplied to the devices.

Today, SRAMs are used as main memory in small systems with high performance like L1 cache (register), and L2 cache (SRAM) memory in microprocessors [4]. Figure 1.1 shows a typical personal computer (PC) microprocessor memory configuration.

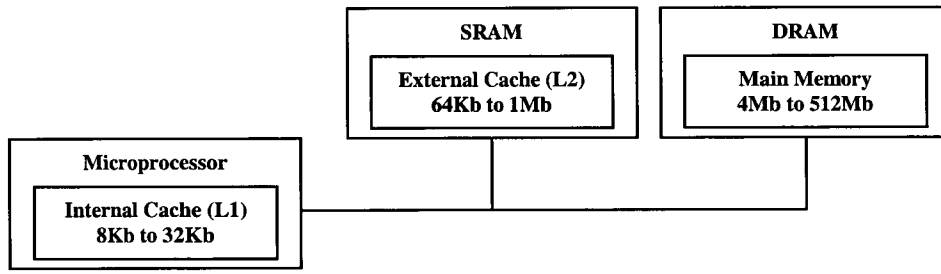

Figure 1.1 : Typical PC microprocessor memory configuration[6].
Source: ICE(Integrated Circuit Engineering)Corporation

Due to the low power consumption, SRAMs have become more and more popular in low power applications. The advantages of CMOS SRAMs are as following:

1. Low supply voltage and low power dissipation compared to DRAMs, due to its small standby current. For mobile devices, battery will have longer lifetime.
2. High noise immunity and high noise margin
3. Simple control logic and easy to use because there is no refreshing circuitry and no address multiplexing.
4. Fast access time.

However, SRAMs have higher cost per bit compared to other technologies [4]. It is also difficult to use internal voltage down converters V_{DC} in low power SRAM. Figure 1.2 shows a general asynchronous SRAM system block diagram.

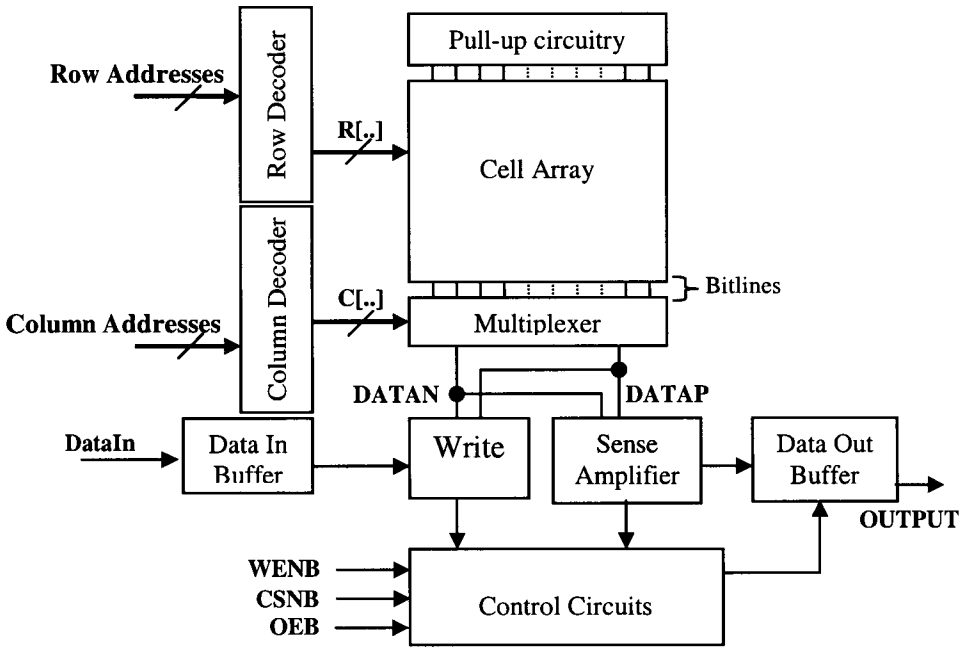

Figure 1.2 : SRAM block diagram.

To perform the read operation, the address bits are placed on the address bus and corresponding row and column of the memory cell or cell in the array will be activated. Then, Chip Select (CSNB) is enabled, followed by Output Enable (OEB). As shown in Figure 1.8a, the data bits are then ready on the data bus. Meanwhile, to perform the write operation, the corresponding row and column of the memory cell will be activated as the read operation. As shown in Figure 1.8b, the Write Enable (WENB) is enabled and followed by data to be written which is fetched from DataIn.

1.3 SRAM History

SRAMs have been developed in three technological paths; bipolar, CMOS and NMOS [1]. Figure 1.3 shows the SRAM technologies development flow chart. Refer to Figure 1.3, each technology has its own characteristics and market demands, which depends on system requirements. Early CMOS SRAMs are in low speed, consume large chip area, and suffered latch-up problem. The first SRAM was developed by using the bipolar technology. The bipolar SRAM has suffered high power consumption and high power dissipation. After the invention of NMOS technology, most of the SRAMs were fabricated using NMOS technology due to its lower power consumption and dissipation. However, research and development have done to enhance the CMOS performance. After the development of polysilicon and aluminium for the CMOS technology, NMOS SRAM technology was replaced. The new CMOS technology has the capacity to implement larger and higher density of CMOS memory cell compared to the