



UNIVERSITI PUTRA MALAYSIA

**DESIGN OF 1K ASYNCHRONOUS STATIC RANDOM ACCESS
MEMORY USING 0.35 MICRON COMPLEMENTARY METAL OXIDE
SEMICONDUCTOR TECHNOLOGY**

YEONG TAK NGING.

FK 2005 54



**DESIGN OF 1K ASYNCHRONOUS STATIC RANDOM ACCESS
MEMORY USING 0.35 MICRON COMPLEMENTARY METAL OXIDE
SEMICONDUCTOR TECHNOLOGY**

By

YEONG TAK NGING

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia in
Fulfilment of the Requirements for the Degree of Master of Science

April 2005



Abstract of thesis presented to the Senate of Universiti Putra Malaysia in
fulfilment of the requirement for the degree of Master of Science

**DESIGN OF 1K ASYNCHRONOUS STATIC RANDOM ACCESS
MEMORY USING 0.35 MICRON COMPLEMENTARY METAL OXIDE
SEMICONDUCTOR TECHNOLOGY**

By

YEONG TAK NGING

April 2005

Chairman : Roslina Mohd Sidek, PhD

Faculty : Engineering

Static Random Access Memory (SRAM) is a high speed semiconductor memory which is widely used as cache memory in microprocessors and microcontrollers, telecommunication and networking devices.

The SRAM operations are categorized into two main groups: asynchronous and synchronous. A synchronous SRAM has external clock input signal to control all the memory operation synchronously at either positive or negative edge of the clock signal. While, in asynchronous SRAM, the memory events are not referred or controlled by the external clock.

In this study, we have proposed an asynchronous SRAM which configured with a self-holding system in the control unit. The self-holding SRAM control system can produce appropriate signals internally to operate the SRAM system automatically, eliminating hold and wait time, and eliminating Sense Enable and Output Enable signals which usually used in SRAM control system. All input



signals are synchronized by the internal control unit. The overall SRAM operations however do not depend on the rising or falling edge of the global (external) clock signal, and thus, the design is still categorized under asynchronous SRAM.

The proposed self-holding control system has been developed for a 1 kilobit SRAM using MIMOS 0.35 micron 3.3V CMOS technology. Due to limited computer resources such as speed and space, the design had been limited to 1 kilobit memory size. The design covers both schematic and layout designs using Hspice and Cadence Layout Editor, respectively. Meanwhile analysis covers Hspice, Timemill and LVS (Layout versus Schematic).

The simulation results have shown the self-holding SRAM control system was working successfully. The design operation speed was 7.0% faster as compared to the SRAM system without the self-holding circuit. An operation speed of 66Mhz with access time of 2.85ns was achieved.



Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

REKABENTUK LITAR TAK SEGERAK 1K *STATIC RANDOM ACCESS MEMORY* DENGAN MENGGUNAKAN TEKNOLOGI *COMPLEMENTARY METAL OXIDE SEMICONDUCTOR* 0.35 MIKRON

Oleh

YEONG TAK NGING

April 2005

Pengerusi : Roslina Mohd Sidek, PhD

Fakulti : Kejuruteraan

SRAM atau "*Static Random Access Memory*" merupakan ingatan semikonduktor yang berkelajuan tinggi di man ia digunakan secara meluas sebagai ingatan utama dalam litar pemprosesan mikro, litar pengawalan mikro, telekomunikasi dan peranti rangkaian.

Operasi *SRAM* dapat dikategorikan dalam dua kumpulan utama, iaitu litar tak segerak and litar segerak. *SRAM* segerak mempunyai kawalan masukan berjam luaran bagi mengawal kesemua operasi secara segerak samada pada pinggir positif atau pinggir negatif. Sementara itu, dalam *SRAM* tak segerak, operasinya tidak merujuk atau dikawal oleh kawalan berjam luaran.

Dalam kajian ini, kami mencandangkan satu litar *SRAM* tak segerak dengan litar pegang-sendiri. Sistem kawalan bagi sistem *SRAM* tersebut dapat menjana keluaran yang sepatutnya secara dalaman bagi mengoperasi *SRAM* secara automatik, menghapuskan masa pegang dan masa menunggu, serta menghapuskan



masukan “Deria Dibenarkan” dan “Keluaran Dibenarakan”. Semua masukan disegerakkan oleh unit kawalan dalaman. Namun, keseluruhan operasi *SRAM* tidak bergantung kepada pinggir positif atau pinggir negatif masukan berjam, dan dengan demikian, ia masih dikenali sebagai *SRAM* tak segerak.

Sistem kawalan yang dicadangkan dibina untuk 1 kilobit sistem *SRAM* dengan menggunakan teknologi MIMOS 0.35 mikron 3.3V *CMOS*. Disebabkan oleh ketersediaan kelajuan komputer dan simpanannya, rekabentuk telah diterhadkan kepada ingatan bersaiz 1 kilobit sahaja. Rekabentuk merangkumi litar dan bentangan dengan menggunakan *Hspice* dan *Cadence Layout Editor* masing-masing. Sementara itu, analisi merangkumi *Hspice*, *Timemill* dan *LVS* (Bentangan lawan Litar).

Simulasi telah menunjukkan sistem kawalan pegang-sendiri *SRAM* tersebut berjaya berfungsi. Rekabentuk tersebut berfungsi dengan 7.0% lebih laju berbanding dengan sistem tanpa kawalan pegang-sendiri. Kelajuan operasi adalah 66Mhz dengan masa capaian bernilai 2.85ns.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my utmost gratitude to my project supervisor, Dr Roslina Sidek, En Rahman Wagiran and En Wan Zuha Wan Hasan for their invaluable guidance, constructive suggestion and encouragement throughout the duration of the project.

My sincere gratitude goes to my sram group in MIMOS Berhad, especially Dr. Mohd Rais Ahmad, En Hanif, En Faizal and Puan Shelli. They have helped and guided me to handle the CAD (Computer Aided Design) tools in MIMOS that were used in the project. Not forgetting my friends Cherk Teing, Kenny and Wai Leong, whose have given me some guidance in the project. And also thanks to staff and consultants of the Engineering Faculty and people who have help my years in University more interesting and meaningful.

Words cannot express my deepest appreciation to my family especially my parents and my wife for their undying love, patient, and support which have enabled me to complete the project successfully.



TABLE OF CONTENTS

	Page
ABSTRACT	ii
ABSTRAK	iv
ACKNOWLEDGEMENTS	vi
APPROVAL	vii
DECLARATION	ix
LIST OF TABLES	xiii
LIST OF FIGURES	xiv
LIST OF ABBREVIATIONS	xx
 CHAPTER	
1	INTRODUCTION 1
1.1	Semiconductor Memories 1
1.2	SRAM 2
1.3	SRAM History 4
1.4	SRAM Market 5
1.5	Publication of Asynchronous Circuits 6
1.6	Types of SRAM 7
1.7	Synchronous SRAMs 9
1.8	Asynchronous (Fast) SRAMs 10
1.9	Asynchronous and Synchronous Issues 11
1.10	Objectives 13
1.11	Thesis Structure 15
2	LITERATURE REVIEW 17
2.1	Types of Semiconductor Memories 17
2.2	Low Power SRAM 18
2.3	Low Power SRAM Design Architecture 18
	2.3.1 Divided Word Line Architecture 19
	2.3.2 Hierarchical Word Line Architecture 21
2.4	SRAM Memory Cells 22
	2.4.1 6T SRAM Cells 23
	2.4.1.1 Conventional 6T SRAM Cell 23
	Architecture
	2.4.1.2 Driving Source-Line 6T SRAM 27
	Cell Architecture
	2.4.2 4T SRAM Cells 29
2.5	Row/Column Decoder 33



2.6	Multiplexer	35
2.7	Sense Amplifiers	36
2.8	Pull-up Circuits	44
2.9	Control Unit	45
2.10	Write Drive Circuit	47
2.11	Input/Output Buffer	47
2.12	Literature Review Conclusion	49
3	METHODOLOGY	50
3.1	Design Flow Chart	50
3.2	SRAM System Block Diagram	54
3.2.1	Inverter	54
3.2.2	NAND/AND Gates	56
3.2.3	NOR/OR Gates	57
3.2.4	SRAM Memory Cell	59
3.2.5	Row/Column Decoder	60
3.2.6	Multiplexer	63
3.2.7	Sense Amplifier	63
3.2.8	Pull-up Circuit	64
3.2.9	Write Circuit	65
3.2.10	Control Unit	66
3.2.11	Output Buffer	70
3.3	Layout Design	72
3.4	Capacitance and Resistance (RC) Effects	74
4	RESULTS AND DISCUSSION	75
4.1	Hspice Analysis Results	75
4.1.1	Inverter and Delay (Inverter Pair)	77
4.1.2	NAND and AND Gates	79
4.1.3	NOR and OR Gates	83
4.1.4	SRAM Cell	85
4.1.5	Row and Column Decoder	87
4.1.6	Multiplexer	89
4.1.7	Sense Amplifier	90
4.1.8	Pull-up	93
4.1.9	Write Drive	94
4.1.10	Control Unit	95
4.1.11	Tristate Output Buffer	98
4.1.12	1K SRAM	99
4.2	Timemill Analysis	103
4.3	Layout	106
4.3.1	Inverter and Inverter Pair (Delay) Layout	106
4.3.2	NAND and AND Gates Layout	108
4.3.3	NOR and OR Gates Layout	111
4.3.4	6T SRAM Cell Layout	113
4.3.5	Row and Column Decoder Input Buffer Layout	115



4.3.6	Row and Column Decoder Layout	116
4.3.7	Multiplexer Layout	116
4.3.8	Sense Amplifier Layout	117
4.3.9	Pull-up Circuit Layout	118
4.3.10	Write Drive Circuit Layout	119
4.3.11	Control Unit Layout	120
4.3.12	Tristate Output Buffer	121
4.3.13	1 Kilobit SRAM System	122
4.4	LVS (Layout Versus Schematic)	123
4.5	Layout Extraction and Analysis	124
4.6	Self-holding System Performance	128
4.7	Characterization	132
4.8	System Expansion Flexibility	133
5	CONCLUSION	137
5.1	Future Development	138
	REFERENCES/BIBLIOGRAPHY	139
	APPENDICES	
A	1K SRAM Hspice Netlist Sample	142
B	LVS Verification Output File (1K SRAM)	151
C	Extracted Spice Netlist Sample	153
	BIODATA OF THE AUTHOR	155



LIST OF TABLES

Table		Page
2.1	Memory types comparison [4].	17
2.2	SRAM cell comparison[16].	23
2.3	Summary of the 6T SRAM cell transistors state refer to node N5 and node N6 condition.	25
3.1	Inverter input and output relation.	55
3.2	A 2-input NAND gate true table.	56
3.3	2-input NOR gate true table.	58
3.4	Addresses decoding (a) Row decoder (b) Column Decoder.	61
3.5	The CSNB and WENB control of the SRAM system.	66
3.6	Inputs and outputs condition for the control unit.	68
3.8	Input and output condition for the tristate output buffer.	71



LIST OF FIGURES

Figure	Page
1.1 Typical PC microprocessor memory configuration [6]. <i>Source: ICE(Integrated Circuit Engineering)Corporation.</i>	2
1.2 SRAM block diagram.	3
1.3 SRAM technologies development flow chart.	5
1.4 SRAM market growth from year 1992 to 2002[7].	6
1.5 Yearly publication count on asynchronous logic[11].	7
1.6 Overview of SRAMs types[6]. <i>Source:ICE, 1997.</i>	8
1.7 Synchronous SRAM timing diagram (a)Read cycle (b)write cycle.	10
1.8a Waveform comparison between conventional SRAM and this project target for the read cycle.	14
1.8b Waveform comparison between conventional SRAM and this project target for the write cycle.	15
2.1 Masahiko Yoshimoto's Divided Word Line (DWL) concept[13].	20
2.2 Hierarchical Word Line (HWL) SRAM architecture[15].	22
2.3 (a) 6T SRAM memory cell configuration, (b) 6T SRAM cell logical representation.	24
2.4 Writing a '1' into 6T cell.	26
2.5 Writing a '0' into 6T cell.	26
2.6 Read a '1' in the SRAM system.	27
2.7 Cell architecture comparison (a) conventional 6T SRAM architecture, and (b) driving source-line 6T SRAM	28



	architecture.	
2.8	Load resistor cell.	30
2.9	TFT (Thin Film Transistor) SRAM cell.	31
2.10	4T full CMOS SRAM cell.	32
2.11	A 4-bit non-pre-decoding circuit.	34
2.12	A 4-bit pre-decoding circuit.	35
2.13	p-channel pass transistor.	36
2.14	n-channel pass transistor.	36
2.15	CMOS pass transistor.	36
2.16	Single ended current mirror sense amplifier [2].	38
2.17	Double ended current mirror sense amplifier [1].	39
2.18	Conventional Current sense amplifier developed by Seevinck[26].	40
2.19	High performance cross coupled current mirror sense amplifier[24].	41
2.20	A hybrid current sense amplifier configuration.	42
2.21	A conventional latch type voltage sense amplifier.	43
2.22	Latch type voltage sense amplifier introduced by Kobayashi et al. [29].	43
2.23	Two MOSFETs pullup circuitries (a)p-channel MOSFETs, (b)n-channel MOSFETs.	45
2.24	Three MOSFETs pullup circuitries with bitlines balancing (a)p-channel MOSFETs, (b)n-channel MOSFETs.	45
2.25	Control unit signaling.	46



2.26	Conventional SRAM write circuit [1].	47
2.27	Power pin protections with input protection pad [36].	49
2.28	A simplified diode model for the ESD protection circuit.	49
3.1	Design flow chart.	51
3.2	The asynchronous self-holding SRAM design block diagram.	54
3.3	(a) Inverter CMOS structure (b) Inverter transit curve.	55
3.4	(a) Inverter pair circuit, (b) inverter pair logical diagram.	55
3.5	(a) A 2-input CMOS NAND gate structure, (b) 2-input NAND gate logical diagram.	56
3.6	AND gate formation with a NAND gate and inverter combination.	57
3.7	A 5-input AND gate (a) CMOS structure (b) logical diagram.	57
3.8	2-input NOR gate (a) circuit diagram (b) logical diagram.	58
3.9	An OR formation.	58
3.10	A 3-input NOR gate (a) schematic diagram (b) logical diagram.	59
3.11	6T SRAM memory cell (a) schematic diagram (b) logical diagram.	60
3.12	The row/column decoder with input buffer circuit.	62
3.13	Pass gate schematic of SRAM Multiplexer.	63
3.14	Single ended current mirror sense amplifier.	64
3.15	Pull-up circuitry.	65
3.16	(a)Write drive circuitry (b)write circuitry waveforms transition estimation.	66



3.17	Self-holding control circuit design for the 1 kilobit SRAM.	67
3.18	The control unit waveforms transition.	70
3.19	Output buffer circuitry.	71
3.20	pMOS transistor (a) Cadence layout (b) cross section view of the pMOS transistor layout.	73
3.21	nMOS transistor (a) Cadence layout (b) cross section view of the nMOS transistor layout.	74
4.1	Spice netlist definition.	76
4.2	A pulse wave waveform definition.	77
4.3	The inverter waveform transition result.	78
4.4	Inverter pair (delay circuit) delay analysis result.	79
4.5	2-input NAND gate transient result.	80
4.6	Illustration shows the root cause of a voltage drops in Figure 4.5.	80
4.7	2-input AND gate transient result.	81
4.8	5-input AND gate transient result.	83
4.9	3-input NOR gate simulation result.	84
4.10	2-input OR gate simulation result.	85
4.11	6T SRAM cell write operation simulation result.	86
4.12	Row and column decoder functionality test result.	89
4.13	Multiplexer functionality test result.	90
4.14	Illustration shows the of the single ended current mirror sense amplifier breakdown.	91
4.15	A modified single ended current mirror sense amplifier.	92



4.16	Modified single ended current mirror sense amplifier voltage swing sensing capability result.	93
4.17	Pull-up circuitry verification result.	94
4.18	Write drive circuitry verification test result.	95
4.19	Control unit functionality test result.	97
4.20	Tristate output buffer functionality test result.	99
4.21	1 kilobit SRAM functionality test result.	101
4.22	(a) Average power consumption	103
	(b) Average current consumption of the 1 kilobit SRAM analysis.	103
4.23	Inverter layout.	107
4.24	An inverter pair or delay circuit layout.	108
4.25	A 2-input NAND gate layout.	109
4.26	A 2-input AND gate layout.	110
4.27	A 5-input AND gate layout.	111
4.28	3-input NOR gate layout.	112
4.29	A 2-input OR gate layout.	113
4.30	6T SRAM memory cell layout.	114
4.31	Duplication and extension of single 6T SRAM memory cell methodology.	114
4.32	Row and column decoder address input buffer layout.	115
4.33	Row and column decoder layout.	116
4.34	Single bit multiplexer cell layout.	117
4.35	A single ended current mirror sense amplifier.	118



4.36	Single bit pull-up circuitry layout.	119
4.37	Write drive circuitry layout.	120
4.38	The control unit circuitry layout.	121
4.39	Tristate output buffer layout.	122
4.40	1 Kilobit SRAM system layout.	123
4.41	1 kilobit SRAM layout functionality analysis result.	125
4.42	1 kilobit SRAM layout functionality test with “chip disabled” after the write cycle.	126
4.43	(a)Average power dissipation (b)Average current consumption analysis of the 1 kilobit SRAM layout.	127
4.44	The 1 kilobit asynchronous SRAM ac characteristic for read cycle (a) without self-holding system, (b) with self-holding system.	130
4.45	The 1 kilobit asynchronous SRAM ac characteristic for write cycle (a) without self-holding system, (b) with self-holding system.	131
4.46	The 1 kilobit asynchronous self-holding SRAM system block diagram.	134
4.47	The 2 kilobit SRAM from the 1 kilobit SRAM expansion configuration.	135
4.48	A 64kilobit asynchronous SRAM system structure which utilizes the asynchronous self-holding SRAM system modules.	136



LIST OF ABBREVIATIONS

μ BGA	Micro Ball Grid Array
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
NMOS	n-channel depletion Metal Oxide Semiconducto
CSP	Chip Scale Package
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
DRC	Design Rules Checker
EEPROM	Electrical Erasable Read Only Memory
ERC	Electrical Rules Checker
ESD	Electro Static Discharge
FBGA	Fine-pitch Ball Grid Array
FeRAM	Ferroelectric Random Access Memory
I/O	Input/Output
IC	Integrated Circuit
LVS	Layout Versus Schematic
LW	Late Write
MRAM	Magnetoresistive Random Access Memory
NMOS	n-type Metal Oxide Silicon
PB	Pipelined Burst
ROM	Read Only Memory
SRAM	Static Random Access Memory
sTSOP	Shrink Thin Samll Outline Package
TFT	Thin Film Transistor
TSOP	Thin Small Outline Package
μ BGA	Micro Ball Grid Array
W/L	Width/Length
ZBT	Zero Bus Turn-around



CHAPTER 1

INTRODUCTION

1.1 Semiconductor Memories

Semiconductor memories have a wide market and commercial values. Semiconductor memories are divided into two families; volatile and non-volatile. Volatile memories are able to retain the data in the device as long as the power is supplied. For non-volatile memories, the data can retain in the device after the cutoff of the power supply. As an example, Read Only Memory (ROM) is a non-volatile memory while Random Access Memory (RAM) is a volatile memory. Recently, combination of volatile and non-volatile memories has been highly applied especially in critical operation such as networking and workstation. Various types of semiconductor memories have been introduced in almost all kind of electrical products ranging from home products to networking and communication products. Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Electrical Erasable Read Only Memory (EEPROM), Double Data Rate DRAM (DDRRAM), Dual Channel DDRRAM, Rambus, Magnetic Random Access Memory (MRAM), Flash memory, Ferro-Electric Random Access Memory, Mirror Bit Random Access Memory, and so on.



Due to the high demand of semiconductor memories for consumers, semiconductor technologies continue to scale down to achieve higher density and higher performance.

1.2 SRAM

Static Random Access Memory (SRAM) is a very fast and low power memory. It consists of latch type cells where refresh circuitry is not required. Refresh circuitry is needed in DRAMs (Dynamic Random Access Memory) to retain the stored data. The refresh system in DRAM requires complex design and engineering sophistication [1]. For SRAM, data are stored in the memory cells as long as voltage is supplied to the devices.

Today, SRAMs are used as main memory in small systems with high performance like L1 cache (register), and L2 cache (SRAM) memory in microprocessors [4]. Figure 1.1 shows a typical personal computer (PC) microprocessor memory configuration.

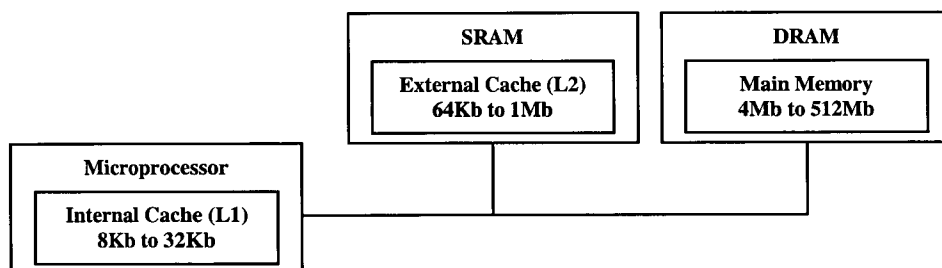


Figure 1.1 : Typical PC microprocessor memory configuration[6].
Source: ICE(Integrated Circuit Engineering)Corporation

Due to the low power consumption, SRAMs have become more and more popular in low power applications. The advantages of CMOS SRAMs are as following:

1. Low supply voltage and low power dissipation compared to DRAMs, due to its small standby current. For mobile devices, battery will have longer lifetime.
2. High noise immunity and high noise margin
3. Simple control logic and easy to use because there is no refreshing circuitry and no address multiplexing.
4. Fast access time.

However, SRAMs have higher cost per bit compared to other technologies [4]. It is also difficult to use internal voltage down converters V_{DC} in low power SRAM.

Figure 1.2 shows a general asynchronous SRAM system block diagram.

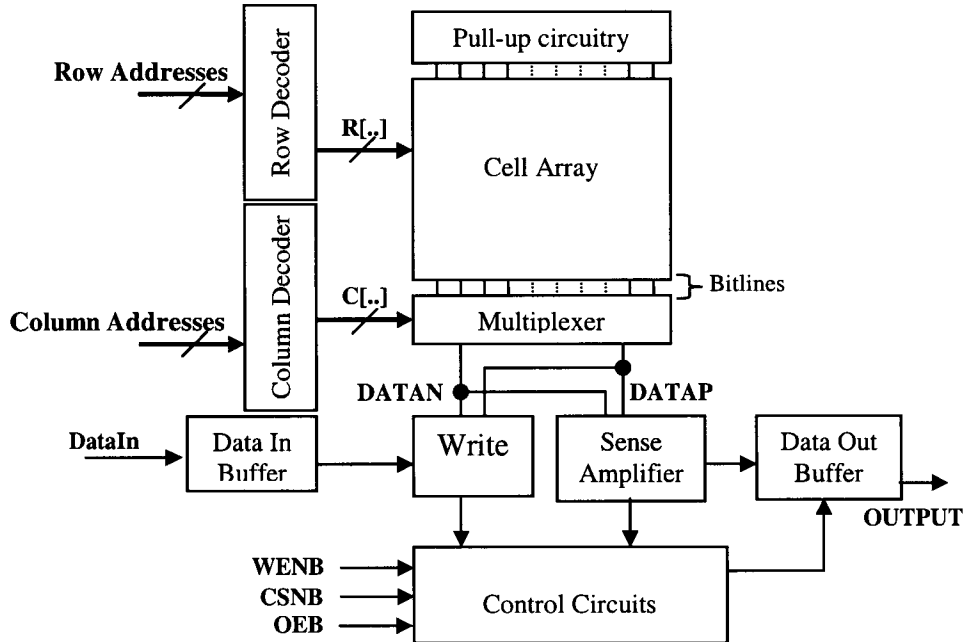


Figure 1.2 : SRAM block diagram.

To perform the read operation, the address bits are placed on the address bus and corresponding row and column of the memory cell or cell in the array will be activated. Then, Chip Select (CSNB) is enabled, followed by Output Enable (OEB). As shown in Figure 1.8a, the data bits are then ready on the data bus. Meanwhile, to perform the write operation, the corresponding row and column of the memory cell will be activated as the read operation. As shown in Figure 1.8b, the Write Enable (WENB) is enabled and followed by data to be written which is fetched from DataIn.

1.3 SRAM History

SRAMs have been developed in three technological paths; bipolar, CMOS and NMOS [1]. Figure 1.3 shows the SRAM technologies development flow chart. Refer to Figure 1.3, each technology has its own characteristics and market demands, which depends on system requirements. Early CMOS SRAMs are in low speed, consume large chip area, and suffered latch-up problem. The first SRAM was developed by using the bipolar technology. The bipolar SRAM has suffered high power consumption and high power dissipation. After the invention of NMOS technology, most of the SRAMs were fabricated using NMOS technology due to its lower power consumption and dissipation. However, research and development have done to enhance the CMOS performance. After the development of polysilicon and aluminium for the CMOS technology, NMOS SRAM technology was replaced. The new CMOS technology has the capacity to implement larger and higher density of CMOS memory cell compared to the