UNIVERSITI PUTRA MALAYSIA

ON-CHIP COMMUNICATION SYSTEM MODELING APPROACH FOR RELIABILITY ANALYSIS FOCUSING ON FUNCTIONAL FAILURES

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Master of Science

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To my loving mother

Sedigheh Behroozfar

And

My best friend in life,

Sama

ABSTRACT

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

ON-CHIP COMMUNICATION SYSTEM MODELING APPROACH FOR RELIABILITY ANALYSIS FOCUSING ON FUNCTIONAL FAILURES

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July 2012

Chairman: Fakhrul Zaman Bin Rokhani, PhD

Faculty: Engineering

The advances in the process technology have shrunk the feature size which has paved the road to higher orders of integration in the recent years. Year by year, the number of components integrated into a single chip is growing. Resulted in larger number of interconnects, the communication between these components is increasingly taking over critical system paths and frequently becomes the basis for performance holdup. Variations of communication and circuit-level techniques are proposed in the literature to facilitate the communication between the on-chip components. While improving communication reliability, power consumption and communication delay are the main concerns of such techniques, most of them are evaluated under unrealistic assumptions about the on-chip communication system. Therefore, the lack of a comprehensive approach for modeling on-chip communication systems is highlighted as the motivation

behind this research. Based on that, a fast and accurate modeling approach inclusive of the impacts of significant contributors to the deep sub-micron noise as well as the dynamic behavior of the receivers is proposed.

This research also investigates the tradeoff between accuracy and computational cost in crosstalk modeling as a part of the modeling approach which has critical impact on the total simulation precision and computational cost. Two algorithms are proposed to control the crosstalk simulation error while minimizing the required computational cost.An adaptive modeling window sizing method, along with an upper bound on the sampling error were applied to guarantee a high order of precision in simulating the crosstalk noise for an RLC interconnect model. The algorithms were verified and the resultsshow that minimum accuracy of 96% is maintained by applying the proposed crosstalk modeling approach while the number of required simulations is reduced by at least factor of 59% for modeling window sizes bigger than 3.

Finally, the significance of using a practical on-chip communication system model is demonstrated through applying the proposed modelling approach to study the impacts of different communication approaches and circuit-level modifications on the reliability performance focussing on functional failures. Using 4-PAM modulation as the signaling scheme together with three variations of Hamming block codes, the proposed on/off-

chip communicationsystem model is compared to AWGN model in terms of bit error ratio. The results confirm that application of simplistic on-chip communication system models like AWGN or primitive crosstalk models leads to inaccurate evaluation of communication techniques while the proposed method is verified to offer a more realistic platform.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

PENDEKATAN PEMODELAN SISTEM KOMUNIKASI DALAM CIP UNTUK ANALISIS KEBOLEHPERCAYAAN DENGAN TUMPUAN KEPADA KEGAGALAN FUNGSI

Oleh

ARASH ABTAHI FOROOSHANI

July 2012

Pengerusi: Fakhrul Zaman Bin Rokhani, PhD

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Kemajuan dalam teknologiproses telah mengecilkan saiz ciri yang telah membuka jalan kepada integrasi di peringkat yang lebih tinggi sejak kebelakangan ini. Tahun demi tahun, bilangan komponen yang disepadukan dalam satu cip semakin meningkat. Keadaan ini menyebabkan bilangan antara sambung yang lebih besar dan komunikasi antara komponen semakin mengambil alih laluan sistem kritikal dan kerap menjadi asas kepada kelambatan prestasi. Variasi teknik pada peringkat komunikasi dan litar telah dicadangkan untuk memudahkan komunikasi di antara komponen atas cip. Dalam meningkatkan kebolehpercayaan komunikasi, penggunaan kuasa dan sela masa komunikasi adalah kebimbangan utama kepada teknik-teknik tersebut dan kebanyakannya dinilai berdasarkan andaian yang tidak realistik terhadap sistem

komunikasi atas cip. Oleh itu, pendekatan yang kurang menyeluruh terhadap pemodelan sistem komunikasi atas cip diketengahkan sebagai motivasi kepada kajian ini. Berdasarkan ini, pendekatan pemodelan yang cepat dan tepat disertai dengan impak penyumbang penting kepada hingar sub-mikron dan juga sifat dinamik penerima dicadangkan.

Kajian ini juga menyiasat hubungan antara kejituan dengan kos pengiraan pemodelan hingar bersilang sebagai salah satu pendekatan pemodelan yang mempunyai kesan kritikal ke atas kepersisan simulasi dan kos pengiraan. Dua algoritma dicadangkan bagi mengawal ralat simulasi hingar bersilang dan dalam masa yang sama mengurangkan kos pengiraan yang diperlukan. Satu teknik permodelan saiz tingkap ubah suai, bersama dengan batas atas kepada ralat persampelan telah digunakan untuk menjamin kepersisan yang tinggi di dalam simulasi hingar bersilang untuk model antara sambung RLC. Algoritma tersebut telah disahkan dan keputusan menunjukkan kejituan minima sebanyak 96% dikekalkan dengan menggunakan pendekatan yang dicadangkan dan dalam masa yang sama bilangan simulasi yang diperlukan dapat dikurangkan kepada sekurang-kurangnya 59% bagi model saiz tingkap lebih besar daripada 3.

Akhirnya, kepentingan menggunakan model sistem komunikasi atas cip yang praktikal telah ditunjukkan melalui penggunaan pendekatan yang dicadangkan dalam mengkaji impak pendekatan komunikasi yang berbeza dan pengubahsuaian di peringkat litar ke atas prestasi kebolehbergantungan dengan tumpuan kepada kegagalan fungsi. Dengan menggunakan modulasi 4-PAM sebagai skim isyarat, bersama dengan tiga variasi kod

blok Hamming, model sistem komunikasi dalam/luar cip yang dicadangkan telah dibandingkan dengan model AWGN dari segi nisbah ralat bit. Keputusan mengesahkan yang penggunaan model sistem komunikasi adalam cip yang mudah seperti model AWNG atau modelhingar bersilang primitif membawa kepada ketidaktepatan penilaian ke atas teknik komunikasi sementara kaedah yang dicadangkan telah dibuktikan dapat menawarkan platfom yang lebih realistik.

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It is needed to also express the heartfelt thanks to my mother who supported me with her patience, care and encouragement during the study. I would also like to express my gratefulness to my friends for giving me a good time here. Lastly, I offer my regards and blessings to all of those who supported me in any respect during the completion of the project.

APPROVAL

I certify that a Thesis Examination Committee has met on (July 2012) to conduct the final examination of Arash Abtahi Forooshani on his thesis entitled "On-chip Communication System Modeling Approach for Reliability Analysis Focusing on Functional Failures" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

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DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institutions.

ARASH ABTAHI FOROOSHANI

Date: 31July 2012

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LIST OF ABBREVIATIONS

BER	Bit Error Ratio
AC	Alternative Current
AWGN	Additive White Gaussian Noise
BER	Bit Error Ratio
C	Interconnect Wire Self Capacitance
Cc	Interconnect Wire Coupling Capacitance
CPU	Central Processor Unit
DC	Direct Current
DNM	Dynamic Noise Margin
DSM	Deep Sub-micron
ECC	Error Control Coding
FEC	Forward Error Correction
FFT	Fast Fourier Transform
GB	Giga Bytes
HDL	Hardware Description Language
ISI	Inter-symbol Interference
L	Interconnect Wire Self Inductance
LSB	Least Significant Bit
M	Interconnect Wires Mutual Inductance
MSB	Most Significant Bit
NM	Noise Margin
PDF	Probability Distribution Function
PWL	Piece Wise Linear

R	Interconnect Wire Resistance
RAM	Random Access Memory
SNM	Static Noise Margin
XOR	Exclusive OR

CHAPTER 1

INTRODUCTION

1.1 Preface

Year by year the human being expects more functionality and speed from the digital devices he uses every day. It was not so long ago that the answer to these demands was simply more number of transistors on a single chip with higher clock frequencies. The industry has been able to shrink the feature size and integrate as many transistors as Moore predicted [1]. The smaller transistors also enabled the predicted space for the frequency increase; however, the constraints on power consumption [2] and the raise in thermodynamic impacts [3] put an end to this trend. The new solution to boost the number of instructions performed per second was to divide the work already done by one processor core and assign it to more number of processors (Figure 1.1).

In the past few years, prototypes of multi-processor units with 48 and 80 cores have been produced by Intel® (Figure 1.2) revealing the challenges in the single chip multi-core design [4]. In the first quarter of 2011, Nvidia® the technology company best known for its graphics processors also introduced Tegra™ 3, a commercial mobile multi-processor series built based on 40nm technology including 12 task specific processors. The number of processor cores on Tegra™ 3 was increased by 4 comparing to its predecessor Tegra™ 2 which was released almost a year before [5].

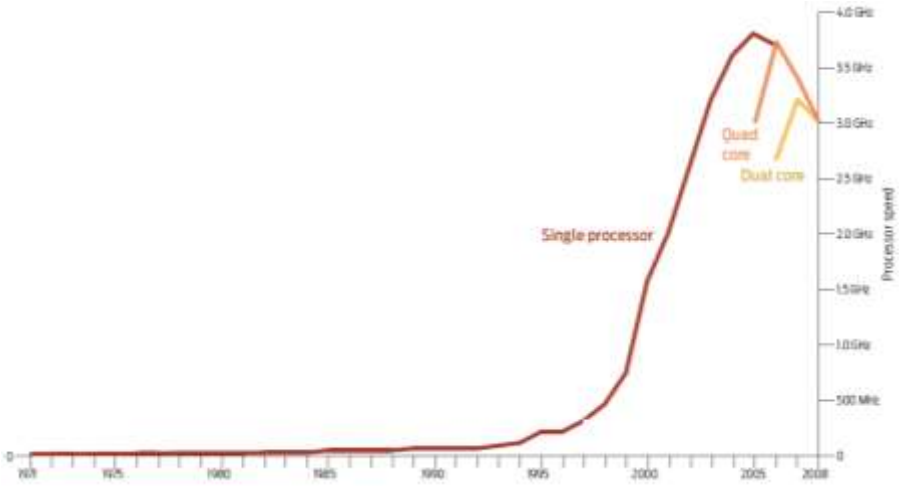

Figure 1.1: Processor Speed Trend [6]

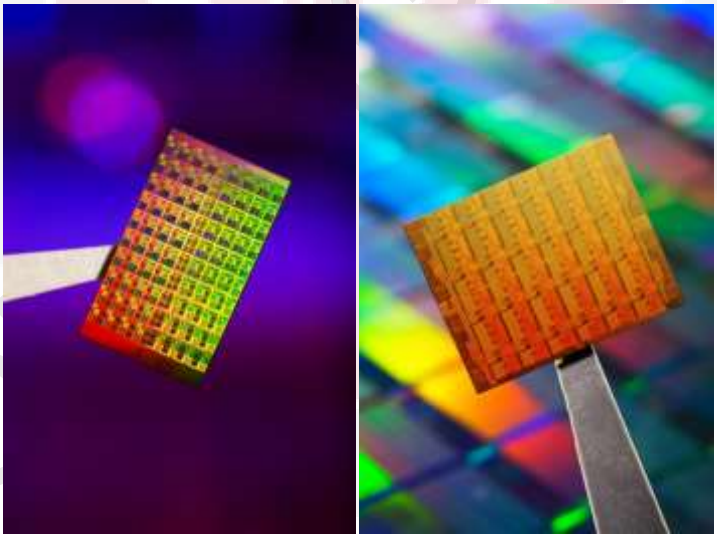

Figure 1.2: Intel 80-core (left) [7] **and 48-core** [8]**Research Chips (right)**

On account of enhancements in process technology, number of components being integrated into a single System-on-Chip is progressively growing. Resulted in larger number of interconnects, the communication between these components is increasingly taking over critical system paths and frequently becomes the basis for performance holdup [9]. In fact, similar to other communication scenarios, the key concerns here are higher data rates, lower energy consumption and further reliability against noise. However, as the feature size and the supply voltages shrink, the signal integrity is getting more and more threatened by the deep submicron (DSM) noise sources on the on-chip interconnects [10]. Moreover, the power consumption of on-chip interconnects can reach up to 50% of the total chip power consumption in new multi-core designs [11].

1.2 Motivation and Problem Statement

Generally speaking, the on-chip communication studies can be branched into two prominent areas (Figure 1.3). First one is concentrated on the communication system modeling and improvement, while the second one concentrated on the communication techniques in charge of improving reliability, speed and or power consumption. The developed models in the first category are supposed to serve the purpose of evaluating the performance of the communication techniques in early stages of design.

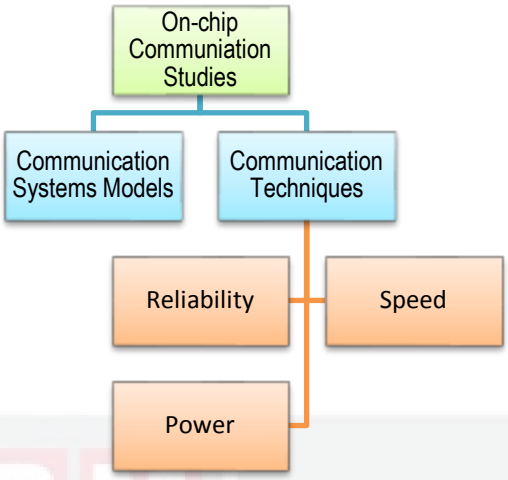

Figure 1.3: On-chip Communication Studies

From the communication point of view, the signals of on-chip interconnect flow from the drivers, through the channel (interconnect wires) to the receivers. Different DSM noise sources have been identified affecting each of these components of the interconnect communication system [12]. These noise sources can result in functional as well as timing failures. Figure 1.4 lists the DSM noise sources.

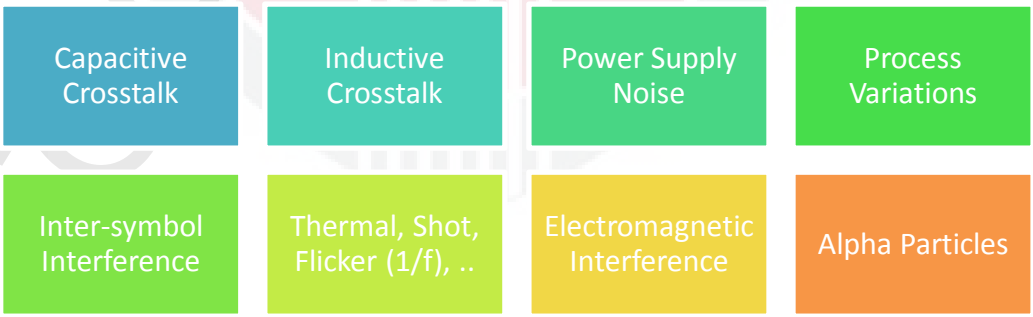

Figure 1.4: Deep Sub-micron Noise Sources[12]

To increase the reliability of the communication system, two approaches have been identified [12]. The first approach is through the *noise budgeting* approach which applies the worst case analysis leading to increase of the noise margin in order to mitigate the noise. This approach results in high signal-to-noise ratio (SNR) at the expense of high power dissipation [13]. The analysis is rather a pessimistic analysis, to consider all noise sources to happen simultaneously at the worst possible extreme value which is misleading in real design.

The other approach is the *fault-tolerant* communication strategy which consists of design techniques that are inherently tolerant to noise and errors. Well-known subcategories under this topic are dynamic noise analysis, bus encoding, and channel coding [10]. These methods have shown great success versus the noise-budgeting approaches in terms of optimality in speed and power [14–16]. However, such communication techniques were largely evaluated through simplistic low-precision channel models which could not show the actual capacity of the techniques.

In order to evaluate the fault-tolerant communication techniques, the very fundamental requirement is a comprehensive model of the communication system which consists of the drivers, receivers and interconnects. Hence, the development of a communication system modeling approach that accounts for the impacts of significant noise sources as

well as the dynamic behaviour of the receiver gates on signal integrity is the most important motivation of this thesis. This research proposes an on-chipcommunication system modeling approach based on superposition principle and sampling theorem that not only is fast enough to evaluate on-chip communication techniques but is also accurate and relatively comprehensive.

1.3 Aim and Objectives

The significance of on-chip communication as well as the demand for practical communication system modeling approaches was highlighted in the past two sections. The main aim of this research is to propose an on-chip communication system modeling approach with focus on functional failures on silent wires which is suitable for evaluating the reliability performance of the on-chip communication techniques. Silent wires are those wires in a bus which their logical state does not alter between two clock periods. These wires are prone to unintended change in their state due to the noise induced by the neighboring transitioning wires also known as aggressor wires. Normally, enormous number of transitions is needed for evaluating the on-chip communication techniques since the techniques are usually designed to minimize the bit error ratio (BER) so that the communication last longer free of errors. Therefore, the objective in this research is to develop a modeling approach which is substantially faster in simulation and imposes less computational costs comparing to circuit-level simulators. Besides, the simulation speed in such an approach should not jeopardize the

accuracy and the model must be accurate enough to provide reliable performance results at the early stages of design. Furthermore, the approach should include the impacts of interconnect wires and the behavior of receivers and be capable of modeling the significant contributors to noise. Note that investigating the impacts of drivers on signal integrity is excluded in this research and a commonly applied method is used to model them. This will be further explained in the third chapter. Furthermore, the dynamic noise analysis at the receiver is expanded from binary to four-level logic.This can open the door to developing such analysis for signaling schemes with higher number of levels. Figure 1.5 illustrates the necessary characteristics of a comprehensive on-chip communication system model.

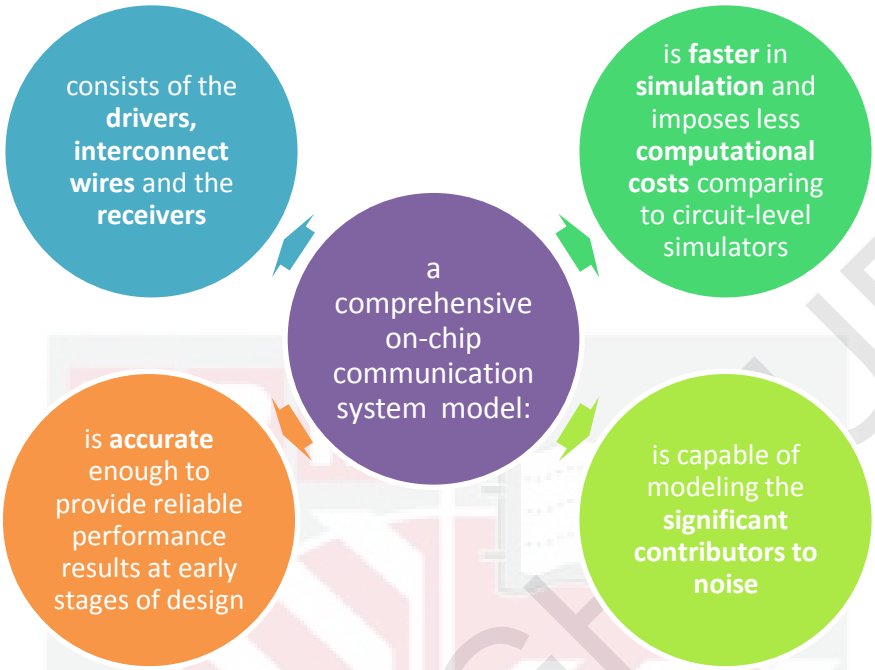

Figure 1.5: The Necessary Characteristics of a Comprehensive On-chip Communication System Model

Including capacitive and inductive crosstalk in the model is a critical task which significantly affects the simulation precision and computational cost. Thus, investigating the tradeoff between accuracy and computational cost in crosstalk modeling is another objective of this research.

The last but not the least, examining the reliability performance of different communication and circuit-level techniques using the proposed modeling methodology is an important goal in this research which allows emphasizing on the significance of using a more realistic on-chip communication system model.

In summary, the objectives in this study are as follows:

1. To propose an on-chip communication system modeling approach with focus on functional failures on silent wires which is computationally fast with high accuracy, suitable for evaluating the reliability performance of the on-chip communication techniques.

2. To investigate the tradeoffs between accuracy and computational cost in crosstalk modelling.

3. To examine the reliability performance of different communication and circuit-level techniques using the proposed modelling methodology.

1.4 Scope of the Work

The proposed on-chip communication modeling approach is focused on simulating the transient behaviour of on-chip metallic interconnects. The accuracy of the modelling approach must be verified against Mentor Graphics Eldo Classic software [17] which is a SPICE accurate circuit simulator. Henceforward, this software is referred to with the term SPICE in interest of readability.

BER is chosen as the criterion for the reliability analysis where the concentration is on functional errors happening on silent wires. Since the on-chip interconnect signal integrity covers a wide scope,the timing errors occurring on transitioning wires are not included in the analysis provided in this researchand the focus is on silent wires. The proposed modeling approach also includes the impacts of the DSM noise on parallel on-chip interconnects and simulates the dynamic behaviour of the receiver circuit on signal integrity.

Also, the selected communication techniques are chosen based on their attributes that help investigating the importance of accurate and fast on-chip communication system modelling. Thus the selection does not necessary represent the best low-power or fault-tolerant communication techniques though their performance is compared with current methods.

Finally, completely random binary data with uniform probability function is generated and used for the reliability and power consumption analysis presented in this work.

1.5 Contributions of the Thesis

In this thesis, the on-chip communication system modeling problem is addressed by proposing an accurate, fast and relatively comprehensive modeling approach. The proposed modeling approach includes the impacts of the channel and the receiver on the signal integrity where its focus is on the functional failures on silent wires.

Moreover, the tradeoffs between accuracy in crosstalk modeling and computational costs are studied. Based on that, twoalgorithmsareproposed to reduce the cost while keeping the accuracy at the desired level. The adaptive modeling window sizing method, along with the upper bound on the sampling error guarantee a high order of precision in simulating the crosstalk noise for an RLC interconnect model.

Eventually, the importance of such modeling approaches in evaluation of communication and circuit-level techniques in the early stages of design is identified through capturing the reliability performance of a low-power signaling scheme with three variations of a fault-tolerant technique.

This thesis is made up of five chapters. The motivation, problem statement, objectives and the scope of the work are stated in the first chapter. Chapter 2 is divided into eight sections which introduce the required background and construct the foundation for the proposed modeling approach. The on-chip communication system modeling approach including dynamic noise margins (DNM) thresholding for 4-PAM is proposed and explained in the third chapter followed by the methodologies for developing the building blocks of the proposed modeling method. Chapter 3 explains the simulation scenarios and the communication techniques used for reliability analysis. The validity of the proposed approach in the third Chapter is evaluated and verified in Chapter 4. Additionally, Chapter 4 presents and discusses the results of the reliability analysis for the simulation scenarios introduced in Chapter 3 and highlights the importance of using more realistic models in exploring the design space. Finally, conclusions of the research and recommendations for future works are presented in the Chapter 5.

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