**Evaluation of optimum scan chain parameter with respect to its power performance of CORTEXM0DS**


ABSTRACT

Design-for-test (DFT) in an integrated circuit is one of essential parts in System-on-Chip. DFT enables testing and debugging of an integrated circuit before it is being produced in high volume. Due to increasing of functionality in advanced nodes of integrated circuit designs, DFT is imperative in reducing defect counts and improving performance of the integrated circuits before reaching the customers. Thus, many research have been done in DFT area in achieving an optimum performance of integrated circuits. Scan test is one of the DFT techniques that enable the integrated circuit design to be tested and debugged. However, due to additional components are being inserted to improve the controllability and observability, high power consumption and dissipation is expected. In this paper, an evaluation of optimum scan chain parameter with respect to its power performance of an integrated circuit will be performed. A block of a microcontroller unit, CORTEXM0DS will be used to where by the scan cells are inserted using DFT Compiler and TetraMAX ATPG from Synopsys. Scan chain from 2 to 20 chains with increment of 2 is simulated and the test power is obtained. The simulation result shows that scan chain with 16 chains count in the design contributed the highest test power of 15.5409 mW while scan chain with 10 chains count result in the lowest test power of 15.2842 mW. The optimum scan chain will also consider the number of test coverage and test pattern.



**Keyword:** Design-for-testability; Scan test; Test power