New tool for converting high-level representations of finite state machines to verilog HDL

ABSTRACT

Automated conversion of high-level representation of Finite State Machine (FSM) to correct-by-construction Hardware Description Language (HDL) is of demand with the increasing complexity of the modern digital controller designs. In this paper, we proposed a tool implementing systematic methodology for conversion and verification of high-level FSM to Verilog HDL. User defined options are provided to increase the flexibility and usability of the tool. MCNC91 benchmarks were used to evaluate the tool performance and correctness. Results indicate that the tool is able to correctly convert all given benchmark circuits with good runtime and memory consumption.

Keyword: Finite state machine; Automation; EDA tool; Conversion