

Variable step size and order strategy for delay differential equations in PIE(CIE)s mode

ABSTRACT

This article deals with the strategy of variable step size and variable order implementation that has been formulated for solving first order of delay differential equations. This strategy is adapted in PIE(CIE)s mode which is generally based on predictor-corrector scheme in multistep block method of order 4 to 9 with s is for convergence test. The purpose here is to enhance the efficiency of the developed predictor-corrector algorithm in the capability to vary automatically not only for the step size, but the order of the method employed as well. All order and coefficients are stored in the code in order to avoid an expensive computational work. The delay argument would be evaluated using Newton divided-difference interpolation at which the points involved would be similar to the current order of the method. Illustrative examples are included to demonstrate the validity and applicability of the presented strategy and comparison is made with the existing results.

Keyword: Delay differential equations; PIE(CIE)s mode; Variable step size variable order