UNIVERSITI PUTRA MALAYSIA

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Master of Science

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Chair: Roslina Mohd Sidek, Associate Professor, PhD

Faculty: Engineering

Neutron detectors are used to detect neutron particles in science, security, and other applications. A typical neutron detection system consists of detector itself and front-end readout electronics. Since neutron detector does not have its operational setting in terms of signal speed and output signal gain, it requires a suitable readout electronics which capable of accepting wide range and fast input signal.

Front-end readout electronics designed in CMOS technology has enabled highly integrated readout channels which increases the resolution of neutron detection. However, due to technology down scaling and the requirements for low power design, the transistor operating region tends to shift from strong inversion to moderate inversion, and the classic MOSFET modelling, also known as "square law" is not applicable anymore. Hence, a more accurate MOSFET modelling is needed in deep submicron CMOS technology to design the front-end readout circuit. Another one significant challenge in designing front-end readout circuit is to design low noise while at the same time minimizing the power consumption. This study presents the design of a low noise and low power front-end readout circuit that is implemented in 130nm CMOS technology. The front-end readout system which has been designed in this study was composed of two parts: (a) pre - amplifier and (b) amplifier pulse shaper.

A simplified Enz Krummenacher Vittoz model or known as EKV model was studied and applied in this work. The model is quite successful in all CMOS operating region, especially in moderate inversion to predict the MOSFET behaviour. The input transistor of front-end system was carefully designed which is critical to readout channel noise performance. A p-channel MOSFET is selected for input transistor due to its lower flicker noise coefficient, and the geometries of all transistors in preamplifier are optimized for minimum noise contribution to the system. The input transistor is made to operate in moderate inversion which is good trade-off between system speed and power consumption. A folded cascode structure is designed for preamplifier to boost the gain and bandwidth. A first order pulse shaper with pole zero cancellation circuit is designed with short peaking time to meet fast counting rate requirements.

A series of simulation including post-layout simulation was carried out to measure front-end system equivalent noise charge, power consumption, charge gain, peaking

time, high counting rate and linearity. Results showed that the front-end readout channel designed in CMOS technology in this work has a good electronic noise performance with only an equivalent noise charge of 183 electrons for a detector capacitance of 1pF. The channel power consumption is only about 0.89mW with a charge gain of 3.6mV/fC. Peaking time is around 104 nanoseconds and it is capable of accepting high count rate input signal of 333 kHz with less than 5% output signal distortion. These results showed that the designed front-end readout circuit implemented in 130nm CMOS technology with input transistor working in moderate inversion has good electronic noise performance, high counting rate while reducing the total power consumption. It also shows that the front-end readout system is suitable for using in neutron particle detection system.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia Sebagai memenuhi keperluan untuk ijazah Master Sains

REKA BENTUK LITAR PEMBACA BERHINGAR DAN BERKUASA RENDAH UNTUK PENGESAN NEUTRON MENGGUNAKAN TEKNOLOGI 130NM CMOS

Oleh

NUERAIMAITI AIMAIER

Mei 2015

Pengersui: Roslina Mohd Sidek, Profesor Madya, PhD

Fakulti: Kejuruteraan

Pengesan neutron digunakan bagi tujuan mengesan zarah neutron dalam bidang sains, keselamatan dan sebagainya. Secara amnya, sistem pengesanan zarah neutron adalah terdiri daripada pengesan neutron itu sendiri dan juga litar pembaca bahagian depan. Oleh sebab pengesan neutron tidak memiliki penetapan operasi dari segi kelajuan isyarat dan gandaan isyarat keluaran, ia memerlukan sistem pemproses elektronik yang sesuai dan mampu menerima isyarat kemasukan yang berjulat lebar dan pantas.

Rekabentuk litar pembaca bahagian depan dalam mod litar bersepadu dengan menggunakan teknologi CMOS membolehkan sistem pemproses elektronik direkabentuk pada skala yang besar serta dapat membantu meningkatkan resolusi pada sistem pengesanan neutron. Walau bagaimanapun, pengecilan skala serta keperluan bagi rekabentuk litar berkuasa rendah menyebabkan kawasan operasi bagi rekabentuk transistor yang akan digunakan beralih daripada penyongsangan kuat ke penyongsangan sederhana, ini menyebabkan pemodelan MOSFET klasik yang juga dikenali sebagai "square law" tidak lagi boleh digunakan. Oleh itu, pemodelan MOSFET yang lebih jitu amat diperlukan dalam teknologi CMOS submikron bagi rekabentuk sistem pemproses elektronik yang akan digunakan dalam litar pembaca bahagian depan. Satu lagi cabaran besar dalam reka bentuk litar pembaca bahagian depan ialah reka bentuk dengan hingar elektronik yang rendah tetapi pada masa masih mengekalkan penggunaan kuasa yang rendah. Kajian ini membentangkan satu rekabentuk sistem pemproses elektronik bagi sistem pengesanan neutron menggunakan teknologi 130nm CMOS. Ia direkabentuk dengan mengambil kira dua parameter penting iaitu; (a) hingar elektronik dan (b) penggunaan kuasa yang rendah.

Model Enz Krummenacher Vittoz yang dikenali sebagai model EKV yang dipermudahkan telah dikaji dan diaplikasi dalam kajian ini dan telah menunjukkan prestasi yang agak berjaya dalam semua CMOS kawasan operasi, terutama dalam penyongsangan sederhana, untuk meramalkan tingkah laku MOSFET. Bahagian transistor masukkan dalam litar pembaca bahagian depan ini telah direkabentuk dengan teliti kerana ia amat kritikal dalam menentukan prestasi hingar elektronik yang akan dijana oleh litar pembaca bahagian depan tersebut. Transistor MOSFET saluran-p telah dipilih sebagai transistor masukkan kerana ia mempunyai pekali hingar kerlipan yang lebih rendah berbanding transistor saluran-n. Geometri bagi semua transistor pada bahagian pra-amplifier telah dioptimakan bagi meminimakan hingar elektronik dalam sistem. Transistor masukkan juga direka supaya beroperasi pada rantau penyongsangan sederhana supaya satu keseimbangan yang baik antara

kelajuan sistem dan penggunaan kuasa dapat diperolehi. Struktur kaskod terlipat telah digunakan bagi rekbentuk bahagian pra-amplifier bagi meningkatkan gandaan dan lebar jalur. Litar pembentuk denyut tertib pertama dengan litar pembatal kutub-sifar telah direka dengan masa puncak yang singkat bagi memenuhi keperluan kadar pembilangan yang pantas.

Satu siri simulasi termasuk simulasi pasca-persediaan telah dilaksanakan bagi mengukur cas hingar setara, penggunaan kuasa, gandaan, masa puncak denyut, kadar pembilangan serta kelinearan sistem. Keputusan kajian menunjukkan bahawa litar pembaca bahagian depan yang direkabentuk dalam kajian ini mempunyai prestasi hingar elektronik yang baik dengan cas hingar setara 183 elektron untuk kemuatan pengesan 1pF. Penggunaan kuasa pula adalah sekitar 0.89mW/saluran dengan gandaan cas sebanyak 3.6mV/fC. Masa puncak denyut yang dihasilkan adalah sekitar 104 ns, ini menunjukkan bahawa ia mampu memproses isyarat kadar tinggi iaitu 333 kHz dengan kurang daripada 5% herotan pada isyarat keluaran. Keputusan ini menunjukkan bahawa reka bentuk litar yang telah direkabentuk dengan menggunakan teknologi 130 nm CMOS dengan transistor masukkan yang beroperasi pada rantau penyongsangan sederhana mempunyai prestasi hingar elektronik yang baik, kadar pembilangan yang tinggi disamping mengurangkan jumlah penggunaan kuasa. Ini juga menunjukkan bahawa litar pembaca bahagian depan ini adalah sesuai untuk digunakan dalam sistem pengesanan zarah neutron.

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I certify that a Thesis Examination Committee has met on 29 May 2015 to conduct the final examination of Nueraimaiti Aimaier on his thesis entitled "Design of A Low Noise Low Power Front End Readout Circuit for Neutron Detection Using 130nm CMOS Technology" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Izhal bin Abdul Halin, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Nor Hisham Hamid, PhD
Associate Professor
Universiti Teknologi Petronas
Malaysia
(External Examiner)

ZULKARNAIN ZAINAL, PhD
Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date: 7 June 2015

This thesis was submitted to the Senate of University Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

Roslina Mohd Sidek, PhD
Associate Professor
Faculty of Engineering
University Putra Malaysia
(Chairman)

Mohd. Nizar bin Hamidon, PhD
Associate Professor
Faculty of Engineering
University Putra Malaysia
(Members)

Nasri Sulaiman, PhD
Senior Lecturer
Faculty of Engineering
University Putra Malaysia
(Members)

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Signature: _____
Name of Member of Supervisory Committee: **Mohd Nizar Hamidon, PhD**

Signature: _____
Name of Member of Supervisory Committee: **Nasri Sulaiman, PhD**

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LIST OF ABBREVIATIONS

FER	Front-end readout
CSA	Charge sensitive amplifier
ADC	Analog to digital converter
CMOS	Complementary metal-oxide semiconductor
MOS	Metal-oxide semiconductor
EKV	Enz, Krummenacher, Vittoz
SNR	Signal to noise ratio
DSP	Digital signal processing
DC	Direct current
NMOS	N-type metal-oxide semiconductor
ASIC	Application specific integrated circuit
PMOS	P-type metal-oxide semiconductor
CR-RC^n	High pass filter followed by n order low pass filter
BPF	Band pass filter
HPF	High pass filter
LPF	Low pass filter
PZC	Pole-zero cancellation
MOSFET	Metal-oxide semiconductor field effective transistor
Si-SiO_2	Silicon and silicon-dioxide
ENC	Equivalent noise charge
ENC_{th}	Equivalent noise charge for thermal noise
$ENC_{1/f}$	Equivalent noise charge for flicker noise
ENC_d	Equivalent noise charge for shot noise
RMS	Root mean square

GBW	Gain bandwidth product
AC	Alternating current

CHAPTER 1

INTRODUCTION

1.1 Research background

The discovery of neutron particle in 1932 was a significant breakthrough in science history, since then neutron science has been developing rapidly all around the world (Bennington, 2014). One of the most significant applications of neutron science is material testing and investigation. The way neutron scattering off gases, liquids and solid matters give scientists information about the structure and composition of these materials which may be widely used in medicine, mining, transportation, building, engineering, food processing and scientific research. In addition, neutrons serve as the complementary probe to X-rays. While X-rays only penetrate materials near surface, neutrons can penetrate most of the materials to depths of several centimetres, which makes it more effective than X-rays (Schaefer & Agamalian, 2004), (Rubio & Gilbert, 2009), (Oed, 2004).

Generally, neutrons can be detected by using helium-3 (^{3}He) filled gas proportional counter. A nuclear reactor ionize the gas inside the detector and generate charged particles. These charged particles are collected by the anode and cathode inside the detector to form a small quantity of current which will be measured by front-end readout circuit as electrical pulses with the amplitude proportional to the neutron energy (Langford, et al., 2013).

1.2 Neutron detection system

Since generated electrical signal in the radiation detector is extremely small, in addition to the detector itself does not have its intrinsic amplification stage, a suitable electrical signal processing channel is required to convert this small charges into a voltage pulse large enough to be processed by next subsequent electronic circuits.

A typical neutron detection system consists of three major blocks: gas filled detector, low noise analog front-end readout (FER) channel, and signal extraction as shown in Figure 1.1. The major function of the detector is to convert the energy released by nuclear reaction to detectable electrical signal.

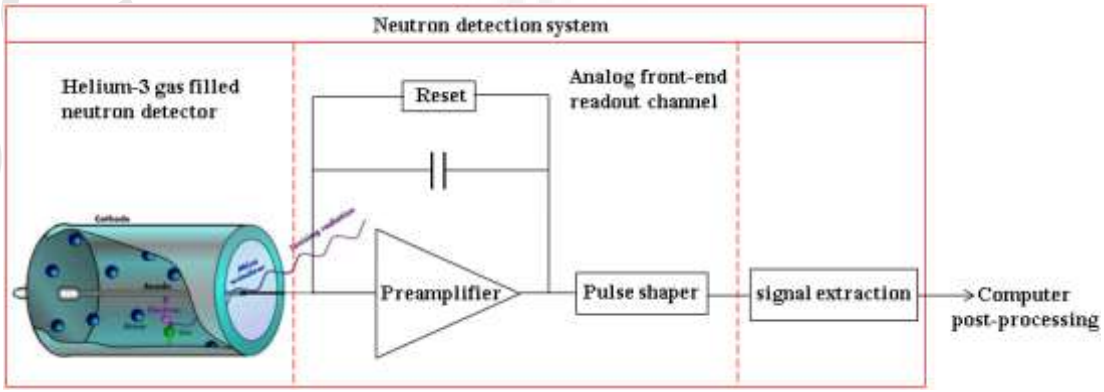

Figure 1.1. The neutron detection system

The FER channel consisting of a charge sensitive amplifier (CSA) and a pulse shaper which convert input charges into voltage pulse then produce a Gaussian-like pulse that carries the information of energy spectroscopy and timing. The signal extraction block may consists of mixed mode circuits such as analog-to-digital converter (ADC), comparator or discriminator, etc. to process the Gaussian-like pulse for peak amplitude and time measurements, and counting rate which is manipulated by computer post-processing (Spieler, 2005).

1.3 Problem statement and motivation

To detect the neutron which is captured in ^{3}He gas filled detector, specific readout electronics is needed. Existing FER electronics are mostly implemented using off-the-shelf op amps (operational amplifiers) and discrete passive components suffers from high power consumption and occupy large area which limits the number of readout channels.

Analog FER electronics based on CMOS technology has power efficiency, occupy only micrometres square area, and is inexpensive. CMOS technology has been adopted to FER circuit since decades though, most of them still limited by noise performance and power consumption. As CMOS technology experiences continues down scaling, accurate MOS transistor modelling is required. This puts challenges to front-end designers to use low power while achieving high signal-to-noise ratio (SNR). Low FER channel power consumption in the range of a few mW is required to minimize the total detector system power consumption.

An efficient CMOS analog circuit design methodology which is using EKV model based on a unified treatment of all the regions of operation of the MOS transistor can be quite successful in terms of low power circuit design where the moderate inversion region is often used because it provides a good trade-off between speed and power consumption. In order to achieve better signal resolution, the signal-to-noise ratio above 125:1 is recommended. Since the time between nuclear radiation events is short, in high counting rate applications, it requires a short peaking time for pulse shaper in the range of a few hundred nanoseconds. Compare to some recent published works (Lombigit, Hamidon, Khalid, & Sulaiman, 2012), (Fang, Hu-Guo, Brasse, & Hu, 2011) and (Noulis, Siskos, Sarrabayrouse, & Bary, 2008) some better design specifications are targeted in this work which are given in Table 1.1.

Table 1.1. The design specifications for the front-end readout channel

Signal-to-noise ratio	Power per channel	Shaper peaking time
125:1	<1 mW	100 ns

1.4 Research objectives

The aim of the research is to design low power consumption and low noise CMOS readout circuits for neutron detectors. The main objectives of this research are:

- To investigate and develop methodologies for optimizing noise in CMOS analog FER circuit
- To design a low noise, low power analog FER circuit with short peaking time using commercial 130nm CMOS technology

- To evaluate the characteristics and performance of the circuit in terms of output gain, electronic noise and dynamic range

The expected major contribution of this thesis is development of a methodology to investigate and optimize noise sources of analog FER circuit to achieve low noise performance while keeping the power consumption as small as possible in deep submicron CMOS technology.

1.5 Research methodology

The research methodology for this work is shown in Figure 1.2. From design specifications the architectures of the FER circuit which consists of charge sensitive amplifier and pulse shaper have been designed. Then schematic captures and simulation (DC, AC, transit, noise) for each block (charge sensitive amplifier and pulse shaper) have been done. After passing the simulations results of each block, the CSA and pulse shaper are integrated to form a FER circuit and a variety of simulations are done to validate the performances of circuit, and redesign has been done if targeted performances are not achieved. The layout of the circuit has been done in IC station and validations of the layout have been done such as design rules check (DRC) and layout versus schematic (LVS). After passing these validation processes, parasitic extraction (PEX) and post-layout simulations have been conducted to ensure the pre-targeted specifications for the FER system are achieved.

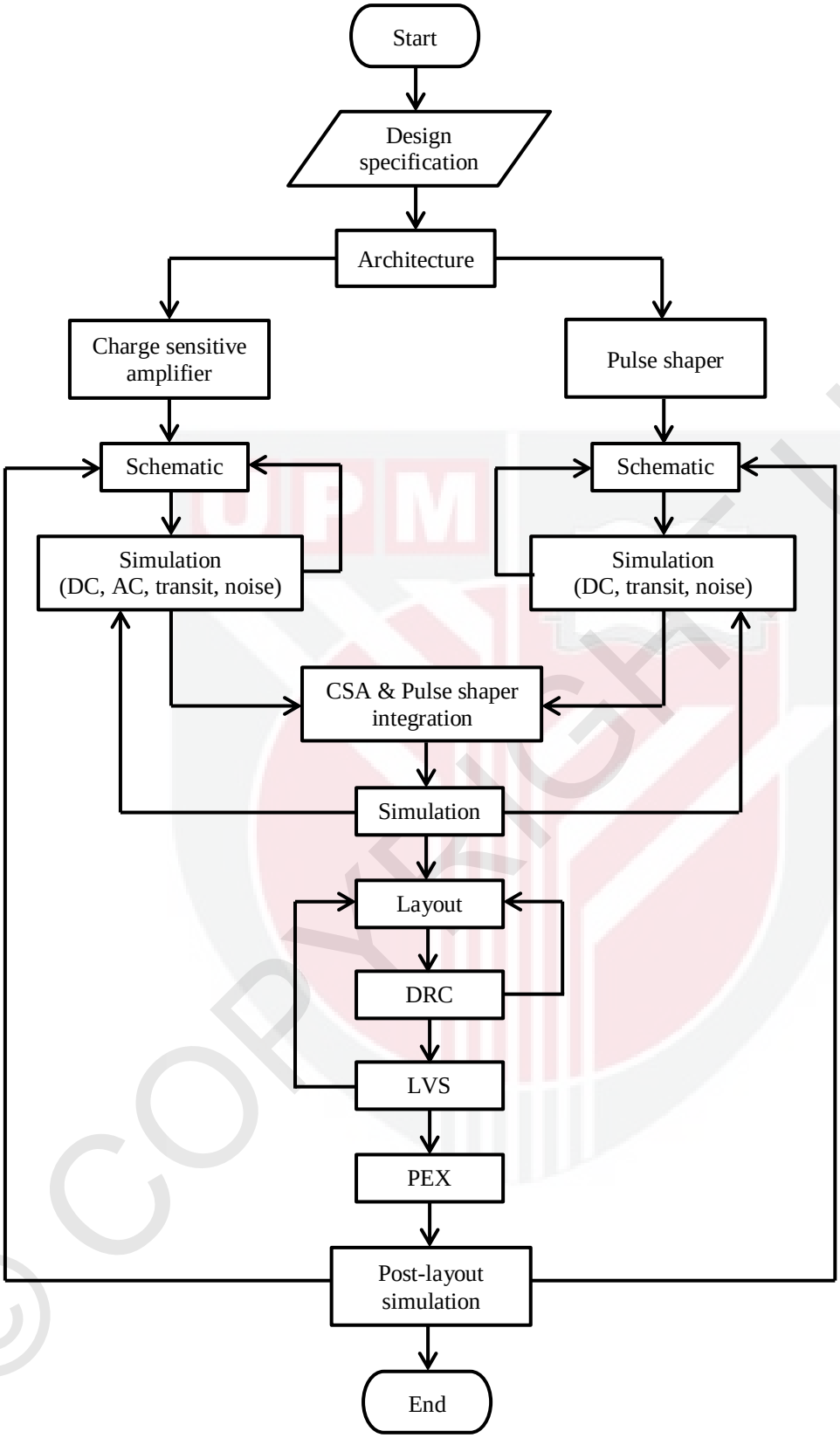

Figure 1.2. The research methodology for this work

1.6 Scope of work

This thesis presents a readout integrated circuit for neutron detector system based on 130nm CMOS technology. The focus of this work is noise optimization for FER circuit. The key tasks are design of low power, low noise, and short peaking time analog FER circuit which consists of charge sensitive amplifier and pulse shaper, evaluate performance of the circuit, and finally design of the CMOS integrated circuit layout.

1.7 Outline of thesis

The thesis is structured in six chapters. Chapter 1 is introduction to research background. Chapter 2 presents a review of literatures of neutron detectors, analog FER electronics and its each component. The detailed design procedure of the charge sensitive amplifier is presented in Chapter 3. Chapter 4 covers design of the pulse shaper. The simulation results, layout design and discussions are presented in Chapter 5. Chapter 6 covers the conclusion of the work and future recommendation.

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