UNIVERSITI PUTRA MALAYSIA

COST - EFFICIENT STANDARD CELL LIBRARY TIMING AND POWER VALIDATION TECHNIQUES

JAAFAR KHADAIR KADAM AL-FRAJAT

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By

JAAFAR KHADAIR KADAM AL-FRAJAT

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

July 2015

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DEDICATION

It is my genuine gratefulness and warmest regard that I dedicate this work to my role model in my life, my father **Prof. Dr. Khadair Kadam Hmood Al-Frajat**. My deepest appreciation should be extended to my mother **Intesar Abdalbaqi**, for withstand the rigors of travel and alienation.

Thanks and glades to my siblings **Ala'a**, **Aseel**, **Ali**, **Zainab**, **Hadeel** and **Fatima** for keeping motivate and support me entire my study period. Although we may be far apart, but we are always close at heart.

"Distance shouldn't matter; at the end of the day, we're all under the same sky"

With love, I dedicate this thesis to all of you.

Thank you.

Jaafar Khadair Al-Frajat

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July 2015

Chairman: Fakhrul Zaman Rokhani, PhD
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A standard cell library contains functional blocks with known electrical characteristics, which are characterized to obtain the following parameters: propagation delay, output transition time, power representation, and capacitance. Standard cell libraries are widely applied by industry designers to the implementation of application-specific integrated circuit (ASIC) designs. Such application is facilitated by the provision of extremely high gate density and excellent electrical performance. Early validation of the characterization data for the standard cells on physical silicon is required to guarantee the correct implementation of the final design in silicon functions. The silicon validation processes correlate the characterized values with the actual silicon performance. However, this process is costly in terms of design and fabrication. Moreover, testing the process on wafer silicon measurement validation is difficult in terms of test time and because of equipment limitation.

In this research, an enhanced silicon validation method was developed to validate the libraries using the basics of the delay chain technique. The method was tested by applying two new approaches to designing test element group (TEG) circuits. These two approaches are sharing load between multi-chains and input control for multi-input gates. These proposed methods can reduce the cost of fabrication through total silicon area reduction of the test chip achieved by decreasing the total number of transistors required in the design. The total number of I/O PADs required in the validation process can also be reduced, and the test time can be enhanced.

The effectiveness of our proposed approaches was evaluated on several test chips that consist of an inverter, a multi-input NAND, and NOR gates as basic cells of combinational logic circuits in the library. Test chips were designed to verify the functionality of the design and to validate timing delays and dynamic and leakage power, which are influenced by cell output loading and cell input transition parameters. The test chip was tested at operating environments that match simulation corners to cover datasheet-specified operating conditions.

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TEKNIK PENGESAHAN MASA DAN KUASA PERPUSTAKAAN SEL PIAWAI YANG KOS - EFISYEN

Oleh

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Perpustakaan Sel Piawai mengandungi bongkah berfungsi dengan ciri-ciri elektrik yang diketahui telah disifatkan untuk parameter-parameter: lengah perambatan, masa peralihan keluasan, perwakilan kuasa dan kapasitans. Dengan menyediakan ketumptan get yang amat tinggi dan prestasi elektrik yang baik, perpustakaan sel piawai telah diterima secara meluas oleh pereka industri dalam pelaksanaan reka bentuk (ASIC) Litar Bersepadu Aplikasi Khusus. Pengesahan data pencirian yang awal bagi sel-sel piawai dalam bentuk fizikal silikon adalah wajib untuk menjamin bahawa reka bentuk akhir dapat dilaksanakan dengan fungsi-fungsi silikon. Proses pengesahan silikon membuktikan bahawa nilai-nilai pencirian adalah memadan dengan prestasi silikon sebenar. Walau bagaimanapun, proses pengesahan silikon ini adalah mahal dari segi reka bentuk dan pemfabrikatan, dan juga sukar dalam pengesahan pengukuran silikon wafer dari segi jangka masa ujian dan pengehadan peralatan.

Dalam kajian ini, kaedah pengesahan silikon yang dipertingkatkan telah dibangunkan dan diuji dengan menggunakan dua pendekatan baru semasa mereka bentuk litar kumpulan elemen ujian (TEG) untuk mengesahkan perpustakaan dengan asas-asas teknik rantaian kelewatan. Kedua-dua pendekatan ialah beban perkongsian antara berbilang rantai, dan kawalan pemasukan untuk get yang berbilang pemasukan. Kaedah-kaedah baru ini dapat mengurangkan kos pemfabrikatan disebabkan oleh pengurangan jumlah keluasan silikon cip ujian dengan mengurangkan jumlah bilangan transistor yang diperlukan dalam reka bentuk. Jumlah pad I/O diperlukan dalam proses pengesahan boleh juga dikurangkan, serta masa ujian dalam proses ujian boleh dipertingkatkan.

Keberkesanan pendekatan yang kami cadangkan telah dinilai pada beberapa cip ujian yang terdiri daripada get penyongsang, berbilang pemasukan TAK-DAN dan get TAK-ATAU sebagai sel-sel asas litar logik bergabungan di dalam perpustakaan Cip ujian telah diuji di persekitaran operasi yang sepadan dengan sudut simulasi untuk meliputi syarat-syarat operasi yang dinyatakan dalam helai data. Perpustakaan sel piawai, Silterra C13LP, telah disahkan dengan menggunakan kaedah ini sebagai kes kajian untuk kajian ini. Keputusan menunjukkan tunda masa dan pengesahan kuasa get penyongsang, TAK-DAN, TAK-ATAU. Semua keputusan dalam simulasi dan wafer silikon memenuhi syarat-syarat operasi untuk sudut proses, voltan dan suhu (PVT).

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TABLES OF CONTENTS

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LIST OF FIGURES

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LIST OF TABLES

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LIST OF ABBREVIATIONS

AMD	Advanced Micro Devices
AMS	Analog Mixed Signal
ASIC	Application Specific Integrated Circuits
ATE	Automated Test Equipment
C	Capacitance
CAD	Computer-Aided Design
CCS	Composite Current Source
CCSM	Composite current source models
CDFII	Cadence Design Framework II
CDL	Circuit Description Language
CEDEC	Collaborative micro-Electronic Design Excellence Centre
CP	Circuit Probe
CSP	Chip-Scale Package
DEF	Design Exchange Format
DLL	Delay Locked Loop
DRC	Design Rule Check
DUT	Device Under Test
ECSM	Effective Current Source Model
EDA	Electronic Design Automation
EDS	Electronic Die Sort
EEPROM	Electrical Erasable Programmable Read Only Memory
ELC	Encounter Library Characterizer
ERC	Electrical Rule Check
FPGA	Field-Programmable Gate Arrays
GDSII	Graphic Design System Information Interchange
GSG	Ground Signal Ground order
HDL	Hardware Description Language
IBM	International Business Machines
IC	Integrated Circuit
IR	Amperes times Resistance (I x R)
IT	Information Technology
KGD	Known Good Die
KTD	Known Tested Die
LEF	Layout Exchange Format
LIB	Liberty

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LSI	Large-Scale Integration
LTAB	Liberty Technical Advisory Board
LVS	Layout Versus Schematic
MEMS	Micro-Electro-Mechanical Systems
MUX	Multiplexer
NLDM	Nonlinear Delay Model
NLPM	Nonlinear Power Model
NMOS	Negative-Channel Metal-Oxide Semiconductor
PDK	Process Design Kit
PEX	Parasitic Extraction
PMOS	Positive-Channel Metal-Oxide Semiconductor
PVT	Process, Voltage and Temperature
R	Resistance
RAM	Random Access Memory
RC	Resistance and Capacitance
ROM	Read Only Memory
SCSP	Stacked Chip-Scale Package
SD	State Dependent
SDPD	State And Path Dependent
SiP	System in Package
SMIC	Semiconductor Manufacturing International Corporation
SPICE	Simulation Program with Integrated Circuit Emphasis
STA	Static Timing Analysis
TEG	Test Element Group
TI	Texas Instruments
TSMC	Taiwan Semiconductor Manufacturing Company
ULA	Uncommitted Logic Array
UMC	United Microelectronics Corporation
USD	United State Dollar
VHDL	VHSIC (Very-High Speed Integrated Circuit) Hardware Description Language
WFT	Wafer Final Test
WLP	Wafer-Level Packaging
WS	Wafer Sort

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CHAPTER 1

INTRODUCTION

This chapter introduces the present research and provides an overview of the design of application-specific integrated circuits (ASIC), including the standard cell library, which forms a main part of early ASIC technologies. This chapter also discusses the problem statement and motivation of the research and presents the objectives and scope of the study. The last section outlines the organization and chapters of the rest of the thesis.

1.1 ASIC Design

As its name indicates, ASICs are non-standard integrated circuits designed for a specific use or application. An ASIC design is generally used for a product with a large production run. The design may contain a huge part of the electronics required for a single integrated circuit. It entails high cost and outcome and is therefore usually reserved for only high-volume products [1]. At the same time, ASICs can be extremely cost efficient for many applications with high volumes; that is, regardless of its cost, a design can easily be obtained to meet the exact requirements of any high-volume products, such as cell phones or other similar applications, particularly high-volume consumer products or widely used business products.

Digital ASICs form a main part of all modern information technology (IT) [2]. Their application in silicon chip technology facilitates the design of complex systems, including wireless devices, smart phones, ts, notebooks, and network routers. The first ASICs dealt only with digital logic functions, whereas modern ASICs have been extended to deal with mixed signals, which can be slotted in both analog and digital logic functions . These mixed-signal ASICs are mostly practical in design and sui for an entire system on chip (SoC), which makes them highly attractive for many modern applications.

Early ASICs used gate array technology. Today, gate arrays are evolving into structured ASICs that contain large IP cores, whereas the logic-only gate-array design is now only seldom implemented by circuit designers [3]. The terms "gate array" and "semi-custom" are synonymous; the former term is usually employed by logic (or gate-level) designers, and the latter by process engineers. By contrast, a full-custom ASIC design defines all the photolithographic layers of a device. It is also used for both ASIC and standard product designs [4].

"Standard-cell" cell libraries, along with modern computer-aided design **(**CAD) systems, are nowadays commonly used for digital-only designs. The standard cell library has a significant performance and accep cost [5]. Moreover, automated layout tools provided by CAD are quick and easy to use and are flexible, but "hand-tweaking" or manually optimizing any performance-limiting aspect of the design is possible.

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1.2 Standard Cell Library

Every ASIC manufacture can create functional blocks with known electrical characteristics, such as propagation delay, power, capacitance, and inductance. These characteristics can be represented in third-party tools [6]. The standard cell design involves utilizing these functional blocks to attain a very high gate density and a verified electrical performance. Any full-custom circuit can be designed completely using only predefined logic cells from a foundry's specific standard cell library and physical design processes, which are provided by standard electronic design automation **(**EDA) tools.

1.2.1 Cell Library Design

The common design flow of a standard cell library is presented in
Figure 1.1. The design is initiated by specifying the widths and lengths of the negative-channel metal-oxide semiconductor (NMOS) and positive-channel metal-oxide semiconductor (PMOS) devices using an analytical approach to meet the design requirements in terms of optimal delay, minimum geometry or optimal noise margins, and drive current [7].

The transistor level schematics for each cell are then generated, and the performance must be verified using circuit simulation tools. After a schematic entry, the layout of each of the cells must be created, such that each cell is as compact as possible, while complying with all the design rules provided by the process foundry. Design rule checks (DRC) and layout versus schematic (LVS) checks must be run to verify the layout. These checks confirm the absence of design rule errors, sizing errors of transistors, or incorrect connections between the layout and schematics.

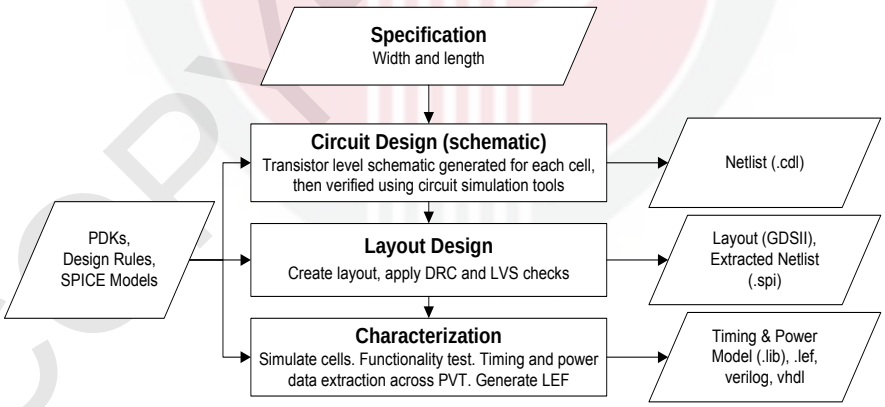

Figure 1.1 Design Flow of The Cell Library

Simulation must also be run on the cells to ensure their proper functionality and to extract their timing and power data. Circuit simulation for data extraction is performed in terms of process, voltage, and temperature (PVT) parameter corners across a range of values expected in usual operations to obtain realistic manufacturing process characteristics [8]. The characterization must be conducted using an automatic cell

characterization tool. After the simulation, the power and timing data are transformed into the format required by the synthesis tool used for the ASIC design.
Along with the library file, the place and route tool also requires a physical description library, which includes definitions of blockages, information on routing layers, pin information to prevent the generation of shorts among the cells when the cell interconnection is being routed [9]. The tool for the abstract generator can be used to obtain the layout exchange format (LEF) file and abstract views for all the cells.

The standard cell library must provide three types of descriptions to be useful to the ASIC designer. These descriptions are provided by the documentation and design files included as a process design kit (PDK) in design tools. These descriptions can be categorized into three groups: (I) physical, (II) logical, and (III) electrical description.

1.2.1.1 Physical Description

The physical description must provide the specific information about the process used for the library, particularly the number of layers in which the metals are processed, the use of each of these layers, and their coordinates (i.e., vertical and horizontal coordinates) [10]. The power rails must also be defined in terms of their width and height. The pins placed and the routing grid must be addressed to facilitate the routing process.

1.2.1.2 Logical Description

In standard cell libraries, three main groups of logic gates co-exist: (1) inverters/buffers, (2) combinational cells, and (3) storage elements (e.g., latches and flip-flops). Given the mostly large number of different logic functions and driving strength options required in typical designs, the largest of the three above mentioned groups is the set of combinational logic gates [11]. The logical description presents the logic functionality of each cell.

1.2.1.3 Electrical Description

The cells must be characterized before the library can be used in the ASIC design. The timing, power consumption, and noise information of each cell are provided by the characterization of the library [12]. Aside from the abovementioned requirements, information on the setup, hold, recovery, and removal time constraints are also presented in the case of sequential cells [13].

1.2.2 Cell Library Characterization

Cell characterization is the process of simulating a standard cell using an analog simulator or an automated characterization tool to extract the timing, power, and noise data and to convert such data into a format that other tools can utilize. The accuracy and reliability of the electrical characteristics of the cells used in a standard cell design environment are crucial to the reliability and accuracy of any design in which such cells are used [14]. However, managing the large amount of information involved is not an easy task. In particular, given that the feature sizes of VLSI chips are increasingly shrinking, maintaining and updating the electrical characteristics of the library elements may adversely affect the process of scaling existing designs to submicron technologies.

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Although the functional and behavioral aspects of the circuit may not change as a result of scaling or moving to a new foundry, timing simulation and critical path analysis become important considerations in porting existing designs into new technologies and foundries [15].

Many types of characterization models are available, depending on the focus of the target characteristics. The nonlinear delay model (NLDM) is widely used to characterize the propagation delay through digital cells and blocks to their outputs depending on the load capacitances and input rise and fall times. The model also describes how the rise and fall times of the output depend on these values. The nonlinear power model (NLPM) focuses more on leakage and dynamic power measurements, aside from timing. The composite current source (CCS) delay model was introduced to address the challenges of modeling technologies with a scale of 90 nm and below. The effective current source model (ECSM) is designed to have accurate model delay, in which voltage fluctuations, process variation, and noise are intensely problematic. ECSM is the industry's first and only open standard current source model and currently enjoys broad industry support.

1.3 Qualification of the Standard Cell Library

A cell library usually consists of an ensemble of hundreds of individual cells. If it is to function as a whole to provide building blocks for larger designs, not only should each individual cell be correctly designed but also should the synthesized designs based on these library cells be free of errors. However, designing a cell library requires conducting many complex tasks and involves the design efforts of a number of engineers. Errors are easily incurred in such situation; even though each cell is designed correctly, errors may still exist. Benchmark circuits are usually designed to uncover leftover errors in a cell library. This way, the quality of a cell library can be substantially improved.

The idea of "high-quality cell libraries" is interpreted in many different ways. A cell library regarded as a high-quality library by one company may not be considered viable by another company [16]. However, high-quality cell libraries possess many common characteristics, some of which are listed below:

1. Each individual cell should function correctly in the models for logic synthesis and simulation.
2. Each individual cell whose timing performance and power consumption are claimed in the data sheet or models should be sufficiently accurate.
3. Each individual cell layout should be free of design rule violations.
4. Each individual cell should be usable by a synthesis tool.
5. The cells should be capable of optimizing the placement and route of a large design.

To achieve these qualification standards, two main fields must be checked in terms of their quality: (1) library verification, or the verification of the applicability of the cells in ASIC tools, and (2) cell validation, or the validation of each individual cell's functionality, timing, and power values as provided by the foundries in the library file.

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1.3.1 Library Verification

The purpose of library verification is to ensure that the cells can work with ASIC tools [17]. This verification is achieved by ensuring that the cells can be utilized in synthesis tools and that they can optimize the placement and route of large designs [18]. The layout of the individual cells must also be free of design rule violations [19]. To justify the cells' capability of being utilized by synthesis tools and of optimizing the placement and route required by a large design, designers must design special benchmark circuits or digital blocks that can address such issues [20]. Using the standard library cells of a design-specified height (i.e., according to the cells used) and the design-specified width of logic rows and varying the width of the wiring channel are various ways of accommodating the number of interconnection wires determined during place and route [21].

1.3.2 Library Cell Validation

A critical issue that affects the standard cell ASIC design is the quality of the standard cells provided by the foundry in the library file [22]. By providing a rich set of library cells, the coordination between the logical and physical design becomes significantly more valuable [23]. However, this process is considered costly in terms of the design of the test chip and the test process. As such, the individual cells themselves must be validated using physical verification DRC and LVS checks to ensure the quality of the layout design. The function of each individual cell must also be checked to guarantee the functionality of the cells [24].

The performance of individual cell is essential to validate the timing and power s provided in the library file. Test element group (TEG) circuits are designed to validate the timing and power on silicon to ensure the match between the silicon and simulation program with an integrated circuit emphasis (SPICE) file [25]. Three types of the TEG circuits have been addressed; the ring oscillator is commonly used to electrically characterize standard cells, although it operates by self-oscillation and catching the oscillation while testing the chip is not easy [26]. The delay path method is very easy to understand and implement, although limited in accuracy [27]. The delay chain method can validate the functionality and performance of standard cell ASIC libraries, facilitates the verification of the performance of each cell, and proves the integrity of the ASIC customer chip design environment [28]. Figure 1.2 shows the validation process for any standard cell design.

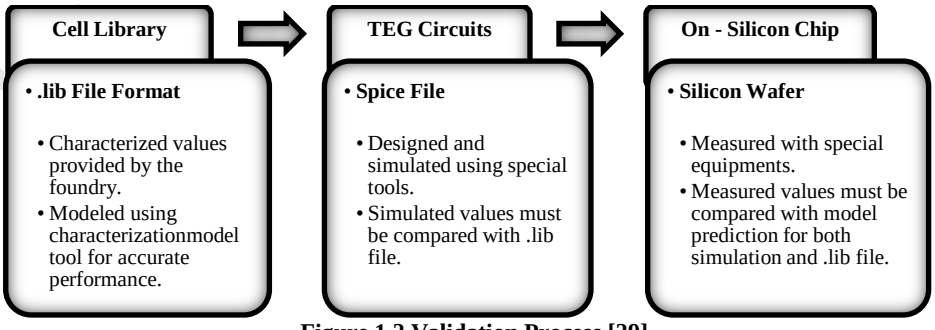

Figure 1.2 Validation Process [29]

1.4 Problem Statement and Motivation

The early validation of the characterization data of standard cells used in physical silicon has become compulsory to guarantee that the final design implemented in silicon correctly functions under all PVT conditions [30-32]. The silicon validation processes prove that the characterized values match the actual silicon performance [27, 32, 33].

However, this process of silicon validation is costly in terms of design and fabrication processes. This cost can be either by consuming large area in the design which will reflect into silicon area later which considered costly, or using huge amount of input/output pins during the design which will lead to have more I/O pads [34-36]. In addition, the process of silicon validation conducting a test on wafer silicon measurement validation is difficult in terms of testing time and limitations in equipment. The time required to validate each individual cell can be long due to the repetition of tests considering different output loads and PVT conditions. Over and above the equipments does not support multi - chain tests at the same time due to the limited number of input/output probes provided by test equipments [33, 34, 36].

1.5 Research Objective

The overall objective of this thesis is to establish an improved validation technique for the standard cell library. Based on the problem statement, the specific objectives of this study are as follows:

1. To design new circuit techniques targeting a cost-effective validation approach of Test Element Group (TEG) circuits.
2. To investigate the trade-off in the performance of the proposed techniques.
3. To examine the proposed validation techniques on transistor-level simulation and on-silicon test chip.

1.6 Research Scope

This work discusses the proposed cost-efficient validation techniques for standard cell libraries. Using TEG circuit approach, and targeting the NLDM-characterized data, the combinational logic cells for Silterra C13LP library is validated to verify the accuracy of the proposed techniques. Many chips using the delay chain method are fabricated and tested in Process, Voltage and Temperate (PVT) corners to obtain a match between the real-silicon and simulated values. The pre-silicon simulation and post-silicon measurement data have been used to validate the library SPICE time and power values. Figure 1.3 shows the scope of the study.

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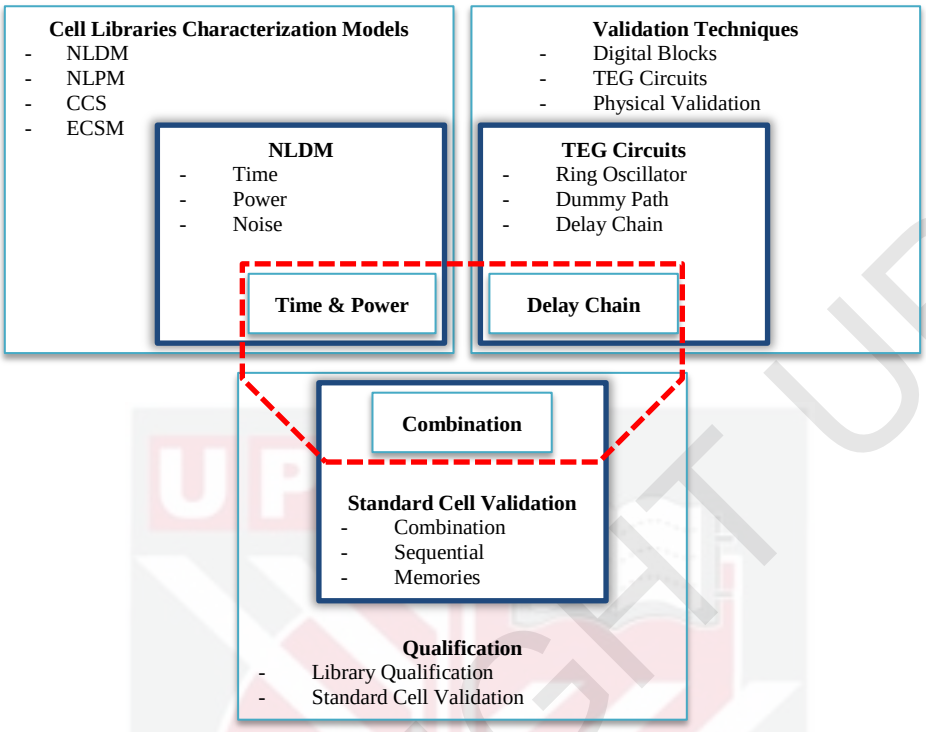

Figure 1.3 Research Scope

1.7 Organization of the Thesis

Chapter 1 provides a general background on ASIC design and defines the standard cell libraries and their characterization. It discusses the qualification of the standard cell library and presents the library verification and cell validation techniques. The rest of chapter explains the problem statement, objectives, and scope of the study.

Chapter 2 reviews in detail the standard cell library validation and discusses the ASIC designs, including the standard cell library, which forms a main part of such designs. It also addresses the characterization models and validation techniques. The last section reviews on-silicon wafer chip measurements and related issues.

Chapter 3 introduces the general methodology of this research and discusses the chip design process. It also discusses the proposed techniques and assumption, which consists of the design, chip, and analytical models. It then describes the simulation and measurements issues.

Chapter 4 presents the results and outcome of the research and analyzes in particular the results of the pre- and post-layout simulation and measurements.

Finally, Chapter 5 summarizes the conclusions suggested by the findings of this research and provides suggestions for future work to improve on the current research.

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