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DEVELOPMENT OF A 115V, 400HZ CASCADED 41-LEVEL INVERTER

AHMAD SYUKRI BIN MOHAMAD

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By

AHMAD SYUKRI BIN MOHAMAD

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To

Alifa Zaireen

Ahmad Syamil Adam

Seri Nur Iman

Abstract of thesis presented to the Senate of Universiti Putra Malaysia
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AHMAD SYUKRI BIN MOHAMAD

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Chair : Prof. Ir. Norman Mariun, PhD

Faculty : Engineering

Cascaded multilevel inverters are widely used in various fields, from oil and gas, power supply installations, to power quality devices. While there are many advantages of the cascaded multilevel inverter such as low voltage stress for each switching device and higher power quality, the main drawback for this type of inverter is the high number of switching device it needs in an installation.

In order to reduce total harmonics distortion (THD) of the output voltage waveform, the number of output voltage level need to be increased, hence the higher number of switching devices. This subsequently increases the installation cost, inverter circuit size and power losses – in the form of heat and voltage losses in the inverter circuit, thus compromises the efficiency of the inverter. In this research, a novel cascaded multilevel inverter topology is proposed with a minimum number of switching devices and driver circuits needed. The proposed topology also needs to turn on only three switching devices at any operation time for any output voltage level configurations.

The prototype inverter can also be designed to supply a load with a specific power factor requirement. Field-programmable gate array (FPGA) is used to replace large number of logic gate circuits that function is to synthesize the switching signals for the prototype inverter from a single oscillator signal. A Verilog program is created in order for the FPGA to produce the desired switching signals according to the design requirements.

The prototype inverter is a single phase 115V, 400Hz 41-level multilevel cascaded inverter designed using the novel cascaded multilevel inverter topology. The prototype inverter is constructed and then tested using resistive and resistive-inductive (RL) loads. In the process, the novel cascaded multilevel inverter topology validity is verified by the simulation and experimental results. The experimental results show that the prototype inverter produces 115V, 400Hz output that resembles a clean sinusoidal waveform with THD of around 2.5% to 3.5%, below the required 5% THD limit according to IEEE standards.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

PEMBANGUNAN PENYONGSANG 41-ARAS BERJUJUKAN 115V, 400HZ

Oleh

AHMAD SYUKRI BIN MOHAMAD

April 2013

Pengerusi **: Prof. Ir. Norman Mariun, PhD**

Fakulti **: Kejuruteraan**

Penyongsang berbilang aras berjujukan digunakan secara meluas di dalam berbagai bidang, daripada industri minyak dan gas, pemasangan sistem kuasa, hinggalah kepada peranti kualiti kuasa. Walaupun terdapat banyak kelebihan penyongsang berbilang aras berjujukan seperti tekanan voltan yang rendah untuk setiap peranti suis and kualiti kuasa yang lebih tinggi, masalah utama untuk penyongsang jenis ini adalah jumlah peranti suis yang tinggi diperlukan dalam setiap pemasangan.

Untuk mengurangkan jumlah herotan harmonik (THD) di dalam bentuk gelombang voltan keluaran penyongsang, jumlah aras voltan keluaran perlu ditingkatkan, menyebabkan pertambahan penggunaan peranti suis. Ini menyebabkan pertambahan kos pemasangan, saiz litar

penyongsang dan kehilangan kuasa – dalam bentuk haba dan kehilangan voltan di dalam litar penyongsang, seterusnya menjejaskan kecekapan penyongsang. Di dalam kajian ini, satu topologi penyongsang berbilang aras berjujukan yang baru dengan jumlah peranti suis dan litar pemandu yang minimum dicadangkan. Topologi yang dicadangkan ini juga hanya perlu menghidupkan tiga peranti suis pada bila-bila masa operasinya untuk apa sahaja tatarajah aras voltage keluaran. Topologi yang dicadangkan ini juga boleh direkabentuk untuk kegunaan beban dengan faktor kuasa yang khusus. Jajaran get dengan medan-boleh-program (FPGA) digunakan untuk menggantikan litar get logik yang besar yang berfungsi menghasilkan isyarat bagi pensuisan prototaip penyongsang daripada isyarat satu pengayun. Satu program Verilog direka untuk FPGA bagi menghasilkan isyarat pensuisan yang diinginkan mengikut keperluan rekabentuk prototaip penyongsang.

Prototaip penyongsang tersebut adalah penyongsang berbilang aras berjujukan satu fasa 115V, 400Hz yang mempunyai 41 aras voltan direkabentuk menggunakan topologi baru penyongsang berbilang aras berjujukan. Prototaip penyongsang ini dibina dan kemudian diuji menggunakan beban rintangan dan rintangan-aruhan (RL). Dalam masa yang sama, kesahan topologi baru penyongsang berbilang aras berjujukan itu ditentusahkan dengan keputusan simulasi dan eksperimentasi tersebut. Keputusan eksperimen menunjukkan prototaip penyongsang ini menghasilkan voltan keluaran 115V, 400Hz yang menyerupai gelombang sinusoid yang bersih dengan THD sekitar 2.5% hingga 3.5%, di bawah had THD 5% yang dibenarkan mengikut standard IEEE.

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I certify that an Examination Committee has met on 8 April 2013 to conduct the final examination of Ahmad Syukri bin Mohamad on his Master of Science thesis entitled "Development of a 115V, 400Hz Cascaded 41-level Inverter" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science degree.

Members of the Examination Committee were as follows:

Wan Zuha b. Wan Hasan, PhD
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Ishak b. Aris, PhD
Professor,
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Suhaidi B. Shafie, PhD
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Soib Taib, PhD
Associate Professor,
School of Electrical & Electronic Engineering
Universiti Sains Malaysia
(External Examiner)

_____
NORITAH OMAR, PhD
Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

Norman bin Mariun, PhD, Ir.
Professor,
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Nasri bin Sulaiman, PhD
Lecturer,
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Mohd Amran Mohd Radzi, PhD
Lecturer,
Faculty of Engineering
Universiti Putra Malaysia
(Member)

BUJANG BIN KIM HUAT, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institution.

AHMAD SYUKRI BIN MOHAMAD

Date: 8 April 2013

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LIST OF ABBREVIATIONS

AC	alternating current
AD	Airworthiness Directives
BJT	bipolar junction transistor
CM	common mode
D	drain terminal (MOSFET)
DC	direct current
EMC	electromagnetic compatibility
FAA	Federal Aviation Administration
FET	field effect transistor
FPGA	field-programmable gate array
G	gate terminal (MOSFET)
GTO	gate turn-off thyristor
HDL	hardware description language
IEEE	The Institute of Electrical and Electronics Engineers
IGBT	insulated gate bipolar transistor
LED	light emitting diode
MEA	more electric aircraft
MOSFET	metal-oxide-semiconductor field effect transistor
Ni-Cad	nickel-cadmium
PCB	printed circuit board
PWM	pulse width modulation
R	resistive

RAT	ram air turbine
RL	resistive-inductive
S	source terminal (MOSFET)
SCR	silicon controlled rectifier
THD	total harmonics distortion
TRIAC	triode for alternating current
VF	variable frequency
VHDL	VHSIC hardware description language
VHSIC	very-high-speed integrated circuits
VSCF	variable speed constant frequency

CHAPTER 1

INTRODUCTION

1.1 Overview

Inverter is one of the most widely used power electronics device in the world today. The application of inverters can be found in three main categories; power supply, motor drives and active filters [1]. Among the many types of inverters, the multilevel inverter is fast emerging as a popular choice in many industrial applications, from oil and gas, power plant to power quality devices [2-3].

The main advantage of this type of power inverter is that it can produce output that is almost resembles the clean sinusoidal output waveform. The staircase output waveform produced by multilevel inverter helps to reduce lower level harmonics while increasing power quality. It also reduces the voltage stress of each individual power switching devices.

Multilevel inverter design concept is where cascaded dc power supplies are connected using semiconductor power switches to synthesize a staircase or stepped voltage waveform. There are several advantages of this design compared with two-level inverter that uses high frequency switching as in the case of PWM technique – the staircase waveform quality means that the output voltage is generated with very low distortion, reduced dv/dt stress and also electromagnetic compatibility (EMC); smaller common mode (CM) voltage therefore reduce the stress on the bearings of a motor connected to a

multilevel inverter; and low distortion in input current drawn by the multilevel inverter [4-9].

Multilevel inverter also can operate in both fundamental switching frequency and high PWM switching frequency. Higher switching frequency however, as in the case of PWM inverter will produce higher switching losses [4, 6].

Other cascaded multilevel inverter advantages are the number of possible output voltage levels is more than twice the number of dc sources [4] and the higher number dc sources or cells are used, the blocking voltage (OFF voltage) requirement of each power switches become smaller – allowing a lower voltage rating power switches used.

The main disadvantage of the multilevel inverter is the high number of power switching devices needed in each design [4-5, 9-10]. This will increase the size of the overall inverter circuit and may increase the space occupied by the inverter in the system. Subsequently, it also increases the power losses in the conducting switches (usually in the form of heat) and also reduces the voltage available at the output terminal due to accumulation of voltage drops across each of the conducting switches. So, it is practical to reduce the number of switches and also the number of conducting switches during inverter operations in order to minimize the heat losses and output voltage drop, as this will increase the overall efficiency of the inverter.

1.2 Problem statement

One of the disadvantages of the multilevel H-bridge is the high number of power switching devices needed in each design [4]. This will increase losses in the circuit as the accumulated losses in each of the turned-on switches increases, along with the increase of the size of the overall inverter circuit and may increase the space occupied by the inverter in the system. Babaei and Hosseini [10], has proposed that the H-bridge topology can be replaced with only two switches for one cell instead of four, plus another four (H-bridge) at the output terminals (to reverse the polarity). This will greatly reduced the number of power switches needed. Although the number of switches is successfully reduced in [10], the amount of switches in the topology and also the number of switches turned-on at any instances of the inverter operation is still considerably high. A new topology can be proposed to further reduce the number of the switches in the overall design and the number of switches needed to be turned-on at any time of the inverter operation.

Another disadvantage of the multicell topology such as the cascaded multilevel inverter is the requirement of independent cells for the inverter input. The favourable design is that the inverter should be supplied with only one dc supply as creating multiple dc outputs from a single dc source will complicate the design. Homeyer et al [11] came up with a design that use transformer to create multiple independent dc supplies for the multilevel inverter. However, the design become quite complicated as the dc supply is converted into ac before being fed to the transformer primary. The transformer secondary is multiple windings and each secondary windings output will be rectified to get multiple dc outputs before being fed into the multilevel inverter to get the desired stepped sine wave.

This dc-to-ac-to-dc-to-ac is expected to increase the harmonics of the output wave. While Esfandiari et al [12-15] improved design using dc-to-ac-to-ac in order to create multiple independent power supplies. The inclusion of the transformer in the design [11-15] means that the weight and size of the whole inverter design will be increased. The multiple conversion stages and the transformer also contribute to the loss and reducing the efficiency of the inverter. Liao et al [16] experimented with capacitors to replace all the independent cells but one, and concluded that capacitor voltage regulation is not achievable in the tested design.

Multilevel inverter also requires quite a high number of switches, as discussed earlier. At any instance during the operation of a multilevel inverter, several power switches need to be operated simultaneously, and this will create some disadvantages such as,

- reduced available voltage at the output terminal due to accumulated voltage drop across all the operating switches,
- relatively high power loss due to accumulated I^2R losses and thermal losses in each switches, and
- high number of components needed in each design.

This thesis will present a novel approach in multilevel inverter circuit design in order to reduce the number of power switches needed and therefore increase the inverter efficiency, reduce losses, minimize the number of components and consequently reduce the inverter size and minimize space consumed.

1.3 Aim and objectives

The aim of this research work is to design and build a cascaded multilevel inverter with a minimum number of switches possible. The inverter will be following the specifications laid in the total harmonics distortion (THD) requirement according to the IEEE standard 519-1992.

In order to achieve the stated aim above, several objectives of this research are set out as below,

1. To design a single phase 400Hz, 115V cascaded multilevel inverter,
2. To create a new cascaded multilevel inverter topology with minimum number of switches and minimum number of conducting switches, and
3. To develop a Verilog program for FPGA that can be used to synthesize cascaded multilevel inverter switching signals and the Verilog program can also be used for other cyclical digital systems

1.4 Scope of work

This research has several limitations:

1. the prototype inverter power supply come from independent dc cells instead of a single-dc-source system,
2. the inverter prototype is consist of only the main inverter circuit, the power switches driver circuits and the switching signal generator circuit,
3. the load used for inverter operational test has a low power, and
4. the load used for inverter operational test is not dynamic load but only passive load – resistive load and complex load with lagging power factors.

1.5 Chapters synopsis

This thesis is divided into five chapters, Chapter 1 – Introduction, Chapter 2 – Literature Review, Chapter 3 – Methodology, Chapter 4 – Results and Discussion, and Chapter 5 – Conclusion.

Chapter 1 briefly discusses the usage and role of inverter in electrical power system, such as in power supply, motor drives and active filters. This chapter describes the issues and problems and also the advantages and disadvantages of the cascaded multilevel inverter. This chapter also states the aim and objectives of this research and the scope of work on how the research is done, particularly the limitations that need to be considered in order to achieve the aim and objectives of the research.

Chapter 2 discusses in details the types of inverters in the electrical power system both from the technology and historical point of view. Apart from that, the chapter also explains the cascaded multilevel inverter topologies, from the conventional cascaded H-bridge multilevel inverter to the currently improved topologies. The advantages and disadvantages of cascaded multilevel inverter also explored in this chapter. The power switching devices and switching signal strategies also briefly mentioned in the chapter.

Chapter 3 describes in details the design process of the prototype inverter, from the design concept to the power devices switching strategy in order to get the correct inverter output according to the electrical power system requirements. The chapter discusses the comparisons of the available cascaded multilevel inverter topologies with the proposed

new cascaded multilevel inverter topology. In doing so, the advantages of the proposed new cascaded multilevel inverter topology are highlighted. The chapter also explains the process of writing the program for the FPGA to transform the FPGA into the switching signal generator for the prototype inverter that design based on the proposed new cascaded multilevel inverter topology.

Chapter 4 shows the results of the functional and operational tests of each module in the prototype inverter based on proposed 41-level new cascaded multilevel inverter topology. The modules are namely the cascaded switching cells (stepped wave synthesizer), the H-bridge, the driver circuit and the switching signal generator circuit (consist of an oscillator and a FPGA). Then the modules are connected in a single assembly and tested to get the inverter output. The test results are shown in the form of tables and graphs. The results are divided into simulation and experimental results, with the simulation results is what are expected, and the experimental result come from the hardware assembly tests. The data then analyzed and discussed.

Finally Chapter 5 summarizes the thesis and relates the results with the objectives stated in Chapter 1, whether the objectives are achieved and how the limitations of the research have any effect on the results and research outcome. Chapter 5 also suggests the future research that can be based on the thesis and improvements that can be made to this research work.

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