A low power multiplexer based pass transistor logic full adder

ABSTRACT

In this paper, a high-speed low-power full adder design using multiplexer based pass transistor logic featuring full-swing output is proposed. The adder is designed and simulated using the industry standard 130 nm CMOS technology, at a supply voltage of 1.2 V. The obtained Power Delay Product (PDP) of its critical path is 29×10-18 J and its power consumption is 2.01εW. The proposed full adder is also capable to function at lower supply voltages of 0.4 V and 0.8 V without significant performance degradation. The proposed adder when cascaded in a 4-bit ripple carry adder configuration, its power, delay and PDP performance are better than the other adders making it suitable for larger arithmetic circuits.

Keyword: Delay; Full adder; Low power; Multiplexer; Pass transistor logic; Power delay product (PDP)