

## **Voltage notch analysis of a taps-based multilevel inverter in the event of one switch failure**

### **ABSTRACT**

There are many advantages of the cascaded multilevel inverter such as low voltage stress for each switching device and higher power quality. One of the drawbacks for this type of inverter is the series switching of the cells it used in its operation. In order to properly operate, all switches must be operational; failure of only one of the switches will result in the failure of the inverter operation. This can be clearly seen in the case of cascaded H-bridge multilevel inverter and other topologies derived from it. In this paper a series cascaded cells taps-based multilevel inverter topology with a minimum number of switching devices and driver circuits needed is discussed. The voltage taps-based topology also needs to turn on only three switching devices at any operation time for any output voltage level configurations. The failure of one of the switches on this topology does not cause total malfunction of the inverter, instead it only causes voltage notches to form on the resulting sine wave output. The notch effect is verified by the experimental results of a prototype single phase 41-level inverter.

**Keyword:** Minimum conducting switches; Multilevel inverter; Notch area; Notch depth; Reduced switching devices